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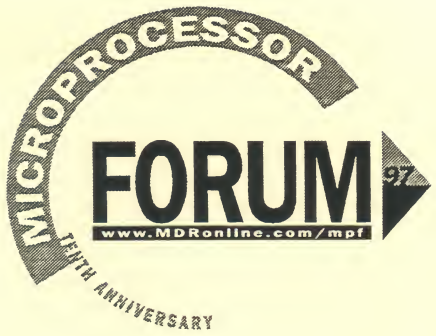
MICROPROCESSOR FORUM 97

presented by MICRODESIGN RESOURCES

CONFERENCE MATERIALS

Fairmont Hotel
San Jose, California
October 14 – 15, 1997



October 13, 1997

Dear Colleague:

Welcome to the Tenth Anniversary Microprocessor Forum. It is your participation that makes the event such a success. To make the most of your time at Microprocessor Forum here are some reminders:

Conference/Seminar Materials
Can be picked up at the materials tables in the Market Street Foyer (conference) and Regency Foyer (seminars). Microprocessor Forum Chip Portfolios are handed out at the beginning of the Literature and Demonstration Center reception in the Regency Ballroom Tuesday evening. Please present the coupons included in your registration envelope to collect your materials. Due to non-disclosure agreements we can not hand out materials in advance of the conference or seminars. Proceedings of the conference and copies of the seminar workbooks are available for sale at the registration area.

Name Badges
Must be worn at all times to gain admittance to Forum events.

Meals
We invite you to join us for complimentary continental breakfast and lunch on conference days and any seminar day you are registered to attend. These meals will be served in the Imperial and Market Street Foyers and in the Regency Ballroom.

Receptions
Please plan to join us for the Microprocessor Forum Receptions. Monday night we offer a welcome reception in the Market Street Foyer. On Tuesday is the grand Literature & Demonstration Center reception where you can pick up your Forum Chip Portfolio and get more information about emerging technologies from 35 participating companies.

Affinity Sessions
Are scheduled for 8:30 Tuesday evening. Sessions on "IA-64 and the Future of Microprocessor Architecture," "The Future of the PC Infrastructure: Socket 7 vs. Slot 1," "The Future of 3D Graphics Acceleration," and "Prospering in New Computing Arenas: Success Beyond Intel's Domain" are slated. More details on these sessions is included in your notebook.

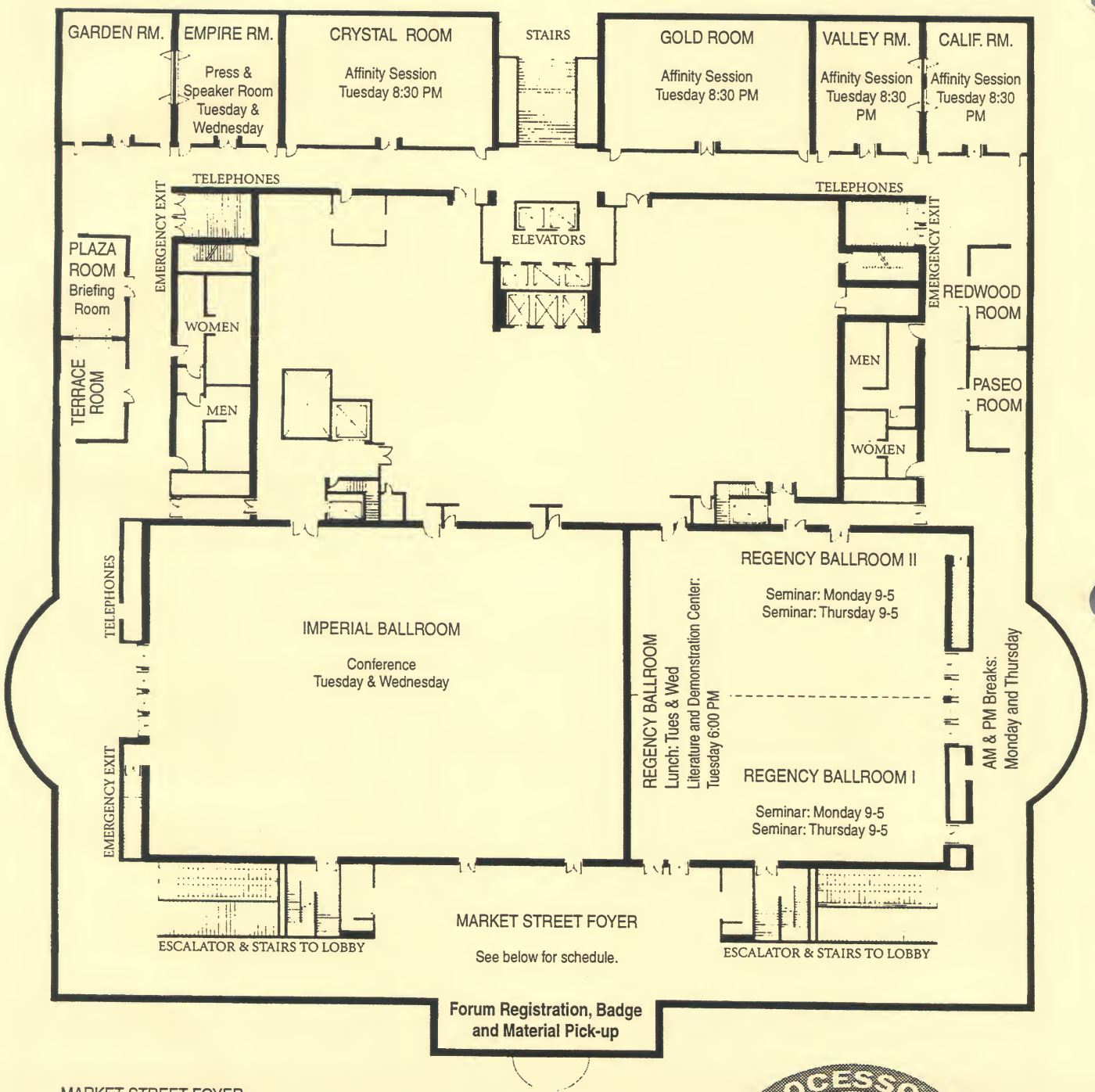
Evaluations
Please take time throughout the conference to fill out the evaluation form found in the inside pocket of your attendee notebook. Completed evaluations will be entered in a raffle for a Sony DVD player and a Palm Pilot PDA.

Need Help?
Just ask anyone wearing a staff ribbon. The MicroDesign Resources team is here to help make the conference more productive and enjoyable for you. Thanks for joining us!

Sincerely,

Michael Slater
Founder and Editorial Director, MicroDesign Resources
Director, Microprocessor Forum

1997 Microprocessor Forum
Event Locations



MARKET STREET FOYER

Continental Breakfast:	Monday—Thursday
AM & PM Breaks:	Tuesday & Wednesday
Lunch:	Monday—Thursday
Reception:	Monday

MICROPROCESSOR FORUM '97
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TENTH ANNIVERSARY

October 13-16, 1997

MICROPROCESSOR FORUM 97
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TENTH ANNIVERSARY

Affinity Sessions

8:30–10:00 pm
Tuesday, October 14, 1997

IA-64 and the future of microprocessor architecture

The emergence of the Intel/HP IA-64 architecture promises to create the biggest shift in the microprocessor landscape in many years. The outline of the technology has begun to emerge, but many questions remain. Join Peter Christy, president of MDR, to discuss issues including:

- How much of a performance advantage over existing RISCs will the IA-64 64-bit instruction set offer?
- What will Merced look like?
- Will this be the crippling blow for the RISC vendors?
- When will it become significant in the x86 PC market?

Crystal Room

The Future of the PC Infrastructure: Socket 7 vs. Slot 1

The split in strategy between Intel and its x86 competitors is fracturing the PC hardware infrastructure. Join industry analyst Bert McComas of InQuest in a discussion of questions including:

- Can Intel drive a rapid migration to Slot 1?
- What will motivate users to make the switch?
- What will the long-term differences in system performance be?
- How long can Intel's competitors keep Socket 7 viable?
- What will Intel's competitors do beyond Socket 7?
- How long will Slot 1 live? What's next?

Valley Room

The Future of 3D Graphics Acceleration

No PC technology is advancing as rapidly as 3D acceleration. The rapid pace of change, varied tradeoffs, and differing agendas among the industry participants has created uncertainty about which approach will be most successful in the coming years. Join Peter Glaskowsky, MDR's 3D and multimedia analyst, to discuss issues including:

- Evolution of 3D benchmarks (with a short presentation from Bill Catchings, ZD Benchmark Operation)
- Is Talisman dead? What is the future for advanced rendering architectures?
- Will geometry processing move off the host processor for mainstream PCs?
- What is the future for OpenGL and other non-DirectX APIs?

California Room

Prospering in New Computing Arenas: Success Beyond Intel's Domain

In the face of Intel's overwhelming success in PCs, many investors are looking at technologies outside of Intel's focus as the best opportunities for building future businesses. Join venture capitalist Andy Rappaport of August Capital to discuss questions such as:

- What are the prospects for non-PC computing devices, including set-top boxes, Web terminals, organizers, and game consoles?
- How far will Intel's reach extend into non-PC arenas?
- What are the architectural and market requirements for successful non-PC computing devices?
- Is this just a place of refuge, or the next big opportunity?

Gold Room

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CONFERENCE PROGRAM

October 14 – 15, 1997
Fairmont Hotel, San Jose

Conference Program Day One

Tuesday, October 14

8:30 **Looking Forward, Looking Back: Welcome to the 10th Annual Microprocessor Forum**
Michael Slater, MDR

Keynote Speech: A New World Order—Alternative Microsoft Windows Platforms
Jerry Sanders, AMD

x86 Microprocessors
Moderator: Michael Slater, MDR

- Competitive Strategies for x86 Microprocessors
  Michael Slater, MDR
- Pentium II Design Enhancements
  Robert Colwell, Intel
- The AMD-K6 Plus: An Enhanced K6 Microprocessor
  Greg Favor, AMD

10:05 **Break Hosted by AMD**

- A New, High-Performance x86 Microprocessor
  Robert Maher, Cyrix
- An Enhanced C6-Family Microprocessor
  Glenn Henry, Centaur Technology
- Panel: Design Challenges for Next-Generation x86 Microprocessors
  All speakers above

11:45 **Lunch Hosted by IBM x86 Microprocessors**

1:00 **The IA-64 64-Bit Instruction Set Architecture**
Moderator: Linley Gwennap

- Motivations and Design Approach for a New 64-Bit Instruction Set Architecture
  John Crawford, Intel and Jerry Huck, Hewlett-Packard
- Q&A
- Intel Architecture Roadmap
  Fred Pollack, Intel
- Panel: Intel Architecture Strategies for High-Performance Computing
  Frank Artale, Microsoft; Steve Chen, Sequent Computer Systems; Les Crudele, Compaq; Dan Glessner, Hewlett-Packard; Russell Holt, NCR; Trey Smith, IBM

Architecture at HP: Two Decades of Innovation
Joel Birnbaum, Hewlett-Packard

3:10 **Break Hosted by Fujitsu**

3:30 **High-Performance RISC Microprocessors**
Moderator: Linley Gwennap

- The Evolving RISC Landscape
  Linley Gwennap, MDR
- Sun's Next-Generation High-End SPARC Microprocessor
  Gary Lauterbach, Sun Microsystems
- A Next-Generation 64-Bit PowerPC Microprocessor
  Mark Papermaster, IBM
- PA-8500: Scaling the PA-8200 With a Large Integrated Cache
  Bill Queen, Hewlett-Packard
- A SPARC Microprocessor for High-End Servers
  Hisashige Ando, HAL Computer Systems
- Panel: Maximizing RISC Microprocessor Performance
  All speakers above, plus Earl Killian, MIPS; Dan Leibholz, Digital Semiconductor

5:35 **Microprocessor Report Awards**
Nick Tredennick, Tredennick Inc.

6:00 **Reception, Literature and Demo Center Hosted by Team MIPS**

8:30 **Affinity Sessions**

Conference Program Day Two

Wednesday, October 15

8:30 **Microprocessors for Embedded Applications**

Moderator: Jim Turley, MDR

- The Changing Face of Embedded Design
  Jim Turley, MDR
- A New, Low-Power Architecture for Embedded Applications
  John Arends, Motorola
- Sun's New microJava Processor
  Harlan McGhan, Sun Microsystems
- A High-Performance, Multimedia StrongARM Microprocessor
  Robert Stepanian, Digital Semiconductor
- An Integrated Pentium-Class Processor for Internet Applications
  Dan O'Neill, National Semiconductor

10:05 **Break Hosted by Motorola**

- A Truly Unified Microcontroller-DSP Architecture
  Rod Fleck, Siemens
- ARM 9TDMI: The Next-Generation Thumb Processor for Higher Performance Applications
  Ian Devereux, ARM Ltd.
- The Hyperstone E1-32X Multimedia Processor for Embedded Systems
  Manfred Schlett, Hyperstone
- Panel: Optimizing Microprocessor Designs for Emerging Embedded Applications
  All speakers above

12:00 **Lunch Hosted by Rambus, Inc.**

1:15 **Next-Generation DRAMs**

Moderator: Peter Song, MDR

- Direct Rambus: The New Memory Standard
  Allen Roberts, Rambus
- Panel: Alternatives for Next-Generation DRAMs
  David Bondurant, Enhanced Memory Systems; Jack Konrath, Fujitsu; Allen Roberts, Rambus; Farhad Tabrizi, SLDRAM Consortium

2:10 **Multimedia Acceleration**

Moderator: Peter N. Glaskowsky, MDR

- Alternatives for Multimedia Acceleration
  Peter N. Glaskowsky, MDR
- A High-Performance x86 Processor with Integrated 3D Graphics
  Doug Beard, Cyrix
- A Mobile 3D Accelerator with Embedded DRAM
  Ronda Collier, S3

3:00 **Break**

- The E4 MPEG-2 Video Codec
  Les Kohn, C-Cube Microsystems
- ManArray Technology: The Scalable Future of Signal Processing
  Gerald Pechanek, BOPS
- Panel: Acceleration Strategies for Multimedia
  All speakers above

4:30 **Panel: Opportunities for Future Microprocessors**

Moderator: Michael Slater
Tom Beaver, Motorola
Les Crudele, Compaq
John Mashey, Silicon Graphics
Fred Pollack, Intel
Andy Rappaport, August Capital
Atiq Raza, AMD

5:30 **Conference Adjourned**

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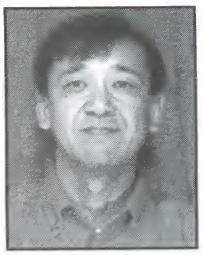
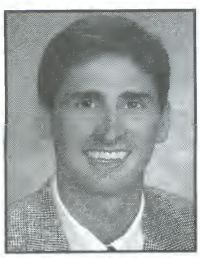
SPEAKER BIOGRAPHIES

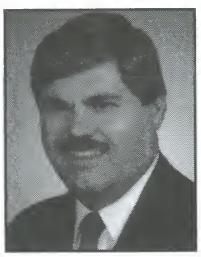


Hisashige Ando
is vice president of processor development of Hal Computer Systems. He's been with Hal for 5 years and has been involved in the development of three generations of SPARC V9 processors.

Joel Birnbaum
is Hewlett-Packard's senior vice president of research and development, and director of Hewlett-Packard Laboratories. He has supervised R&D teams responsible for RISC architecture at HP and IBM.

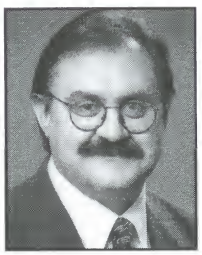


John Arends
area of expertise at Motorola has been RISC microprocessor design and implementation, including both 88000 and PowerPC. His current focus centers around the development of a new low-power high-performance microprocessor architecture for embedded applications.



David Bondurant
is director of marketing and applications for Enhanced Memory Systems. He is responsible for strategic and tactical marketing, applications engineering, marketing communications, and public relations.

Douglas Beard
is MX microprocessor design manager at Cyrix Corporation, which he joined in 1993. Previously he was with Supercomputer Systems as chief hardware architect and hardware design group manager, and with Gould Computer Systems Division as project manager.

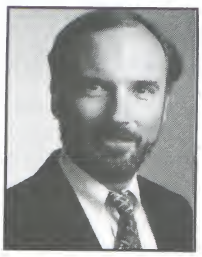


Peter Christy
took over the reins as president of MicroDesign Resources in 1996. He directs all aspects of the company including operations, business planning, product development, marketing, and new business development. He also contributes on computer trends and marketing for *Microprocessor Report.*

Thomas Beaver
is corporate vice president and director of marketing and sales with the networking and computing systems group at Motorola's semiconductor products sector. In his 32 year career with Motorola, he has held various positions within the company.

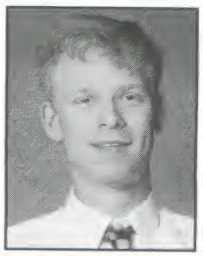
Ronda Collier,
engineering manager for the mobile products group at S3, is responsible for mobile graphics products from definition through implementation. She also manages the design team, as well as interfacing with the marketing and central engineering organizations.

Robert Colwell
manages the architecture team that is designing the next-generation processor within the Microprocessor Development Division at Intel's Hillsboro, Oregon facility. He joined Intel in 1990 as a senior architect on the P6 project, and became manager of the architecture group two years later. In 1996 he was named an Intel Fellow.

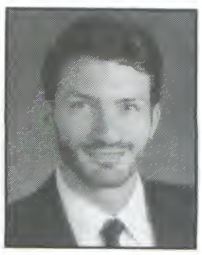


John Crawford
is the director of microprocessor architecture at Intel. He manages the development of future microprocessor architectures, and the development of the simulation tools necessary to validate functional completeness and performance.

Lester Crudele
is vice president and general manager of the workstation division in the enterprise computing group at Compaq Computer Corporation. He is responsible for driving the product development, strategy, and vision for the workstation division, including engineering, sales, and marketing.



Ian Devereux
is the chief engineer of the ARM940T development. He joined Advanced RISC Machines in 1995 and has been a major contributor to the development of the ARM8 and ARM9TDMI processor families.

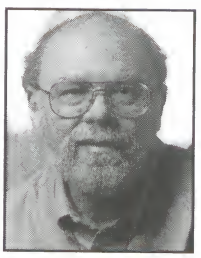


Greg Favor
is a senior fellow at Advanced Micro Devices, where he is responsible for future x86 processor architecture development efforts. Prior to this, he was chief processor architect and then director of K6 processor development.

Rod Fleck
is director of the 32-bit microcontroller group at Siemens Components, where he's been an engineer and technical manager since 1984. He worked on the development team for AMD's 29000 architecture, defined Siemens' 16-bit architecture, and was director of hardware/software coverification at Synopsys.

Peter Glaskowsky
is senior analyst of 3D and multimedia technology for MicroDesign Resources and is one of the industry's leading graphics analysts. He came to MDR from Integrated Device Technology, where he was a chief engineer in the systems technology group.

Linley Gwennap
is editor in chief and publisher of *Microprocessor Report* and director of product development for MicroDesign Resources. He joined MDR in 1992 after eight years at Hewlett-Packard working on RISC systems.



Glenn Henry
has been president of Centaur Technology since April, 1995. Previously, he was a consultant to MIPS Technology (SGI) as well as the chief technology officer and senior vice president of the product group for Dell Computer Corporation.

Jerry Huck
is the manager of processor architecture within Hewlett-Packard's computer organization. His time is divided between managing a small team responsible for processor simulators, platform architecture definition, and participating in the joint definition of processor architecture with Intel.

Earl Killian
is director of architecture for MIPS Technologies. Previously, he cofounded Quantum Effect Design, participating in developing the R4600, R4650, and R4700 MIPS RISC processors.

Les Kohn
is a C-Cube fellow and chief architect of the DVx product family. Prior to joining C-Cube, he was the chief architect for Sun's UltraSPARC and Intel's 860 processors.

Jack Konrath
is director of strategic marketing for memory products at Fujitsu Microelectronics. Most of his 28 years of experience have been in semiconductor memory-related positions, the rest in core logic and graphics.

Gary Lauterbach
is distinguished engineer and chief architect for the UltraSPARC-III microprocessor at Sun Microsystems, and is responsible for research, design, and development of high-performance processors.

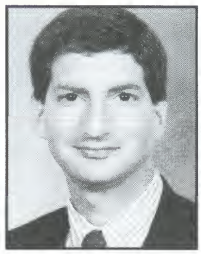
Daniel Leibholz
is a microprocessor architect in the semiconductor division of Digital Equipment Corporation, where he architected major sections of the Alpha 21264. He has interests in the areas of processor architecture, performance analysis, and system design.

Robert Maher
is vice president of engineering at Cyrix Corporation and is responsible for future processor designs. One of Cyrix's initial design engineers, he was project director for the Cyrix 5x86 processor, and was responsible for development of the M2 processor.

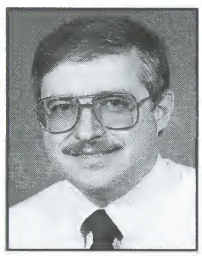
John Mashey
is director, systems technology in Silicon Graphics R&D. He's an ancient UNIX person, having started work on it at Bell Labs in 1973. He has worked on and managed projects in both commercial and technical computing, helped design the MIPS architecture, and was also one of the founders of SPEC.

Harlan McGhan
is the technical marketing group manager for the Sun Microelectronics volume products division. In addition to serving as a principal evangelist for Sun's new line of JavaChips, he focuses on high-level product planning, market requirements, and new product definitions.

Dan O'Neill
is director of National Semiconductor's integrated processor unit, which develops and markets x86-based functionally integrated products. He started the unit in 1993.



Mark Papermaster
is project manager for the POWER3 microprocessor at IBM. He has worked for 15 years in microelectronics and microprocessor engineering, including as manager of circuit and physical design for the PowerPC 601 microprocessor.



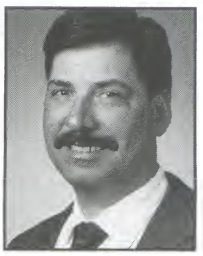
Gerald Pechanek,
inventor of the ManArray, is chief technical officer and cofounder of BOPS. He has over 25 years of development experience.

Fred Pollack
is the director of the measurement, architecture, and planning group at Intel. He directs the planning for Intel's future microprocessors. His group is responsible for all Intel core platform architecture and performance analysis.

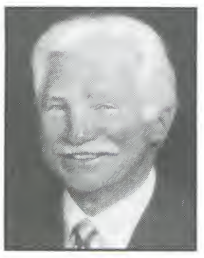
Bill Queen
is a project manager for the PA-8500 design in Hewlett-Packard's Microprocessor Lab in Fort Collins, Colorado. He previously worked on the PA-8000 and PA-7100LC.

Andy Rappaport
is a general partner at August Capital. An oft-cited authority on semiconductor and hardware design technologies, he has written and lectured extensively on the changing structure of the semiconductor, computer, and telecommunications equipment industries.

S. Atiq Raza
is senior vice president and chief technical officer, as well as a member of the board of directors for AMD. Prior to the merger of Advanced Micro Devices and NexGen, he was the president and chief executive officer of NexGen.

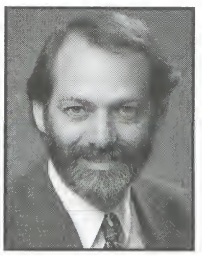


Allen Roberts
is vice president and general manager of the memory and technology division of Rambus. Prior to joining Rambus, he served as director of high-end engineering at MIPS.

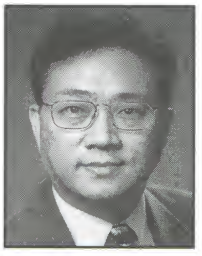


W.J. (Jerry) Sanders III
is chairman of the board and chief executive officer of Advanced Micro Devices. He cofounded the company in 1969 with seven others and has been CEO since its inception.

Manfred Schlett
joined hyperstone in 1993. He was responsible for the DSP concept of the E1-32 RISC/DSP architecture and is now project manager for the European consortium EURICO developing the next hyperstone RISC/DSP generation.

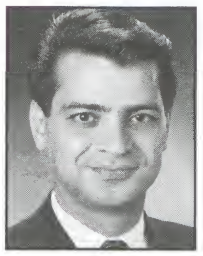


Michael Slater
is founder and principal analyst of MicroDesign Resources, editorial director of *Microprocessor Report*, and program director for Microprocessor Forum. He was previously an independent engineering consultant and an R&D engineer at Hewlett-Packard.

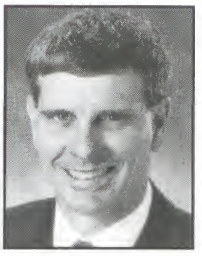


Peter Song
is senior analyst for MicroDesign Resources and senior editor of *Microprocessor Report*. He contributes analysis of high-performance microprocessors. He joined MDR from Samsung, where he was a senior manager and principal engineer.

Robert Stepanian
is a senior computer architect with Digital Equipment Corporation, involved in the architecture definition of the StrongARM processor with the programmable media unit.



Farhad Tabrizi
is chairman of the SLDRAM Consortium and director of strategic marketing at Hyundai Electronics. At Hyundai, he is responsible for setting strategic directions for future memory products.



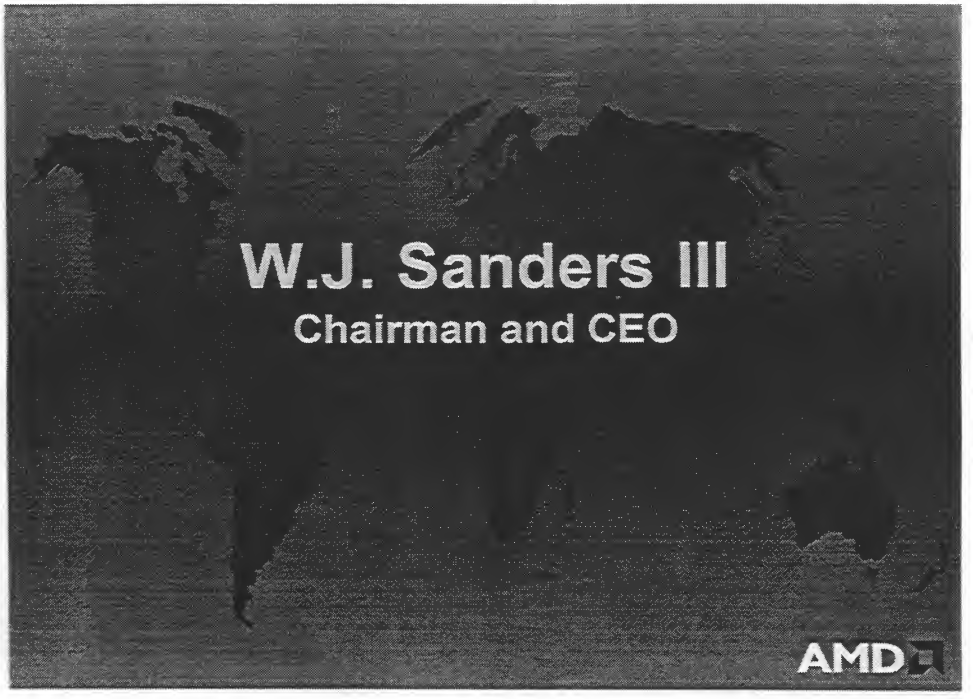
Nick Tredennick
would like to be president of TechNerds International. He has patents, publications, experience, and the usual degrees, but is having trouble connecting "does well" with "pays well."

Jim Turley
is senior analyst and senior editor of *Microprocessor Report* specializing in high-performance embedded microprocessors. He joined MDR in 1994 after devoting more than a dozen years to design engineering, engineering management, product marketing, and program management.

Keynote: A New World Order— Alternative Microsoft Windows Platforms

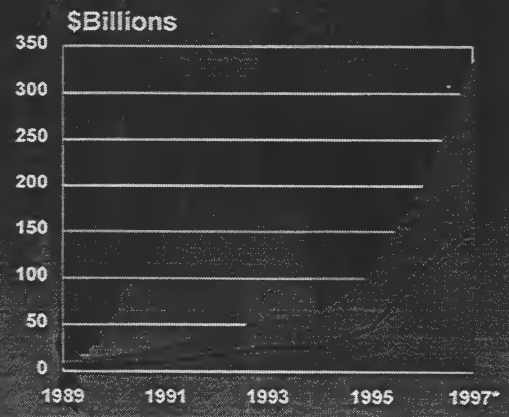
Jerry Sanders, *AMD*

presented by MICRODESIGN RESOURCES


W.J. Sanders III
Chairman and CEO
AMD


A New World Order -
Alternative Microsoft
Windows Platforms
October 14, 1997
AMD

Combined Intel/Microsoft Market Value 1989-1997



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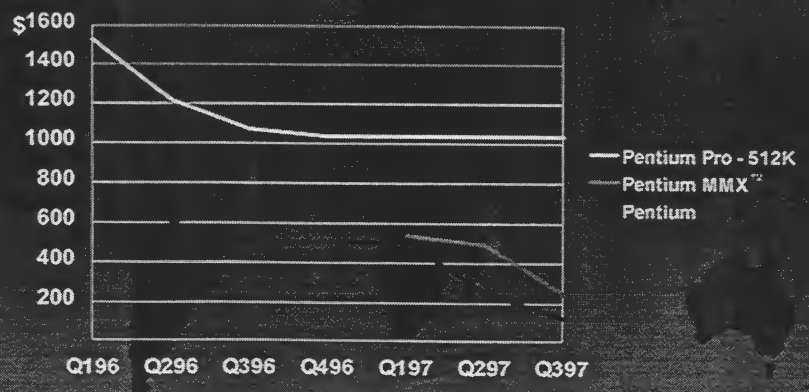
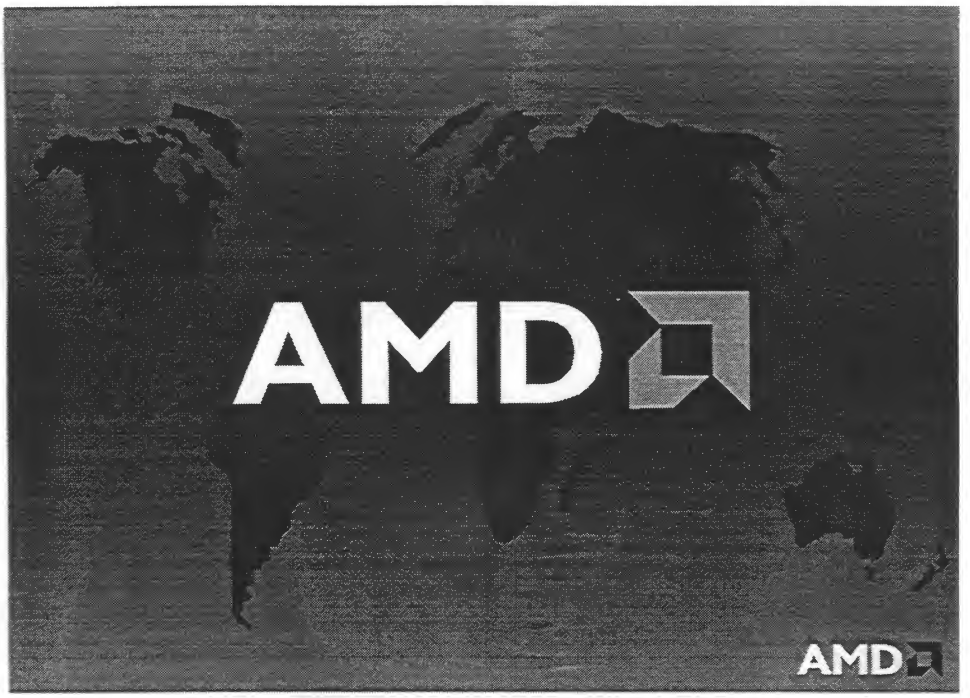
AMD

Intel 1K Pentium Pricing @ 200MHz



Source: Microprocessor Report

AMD


AMD
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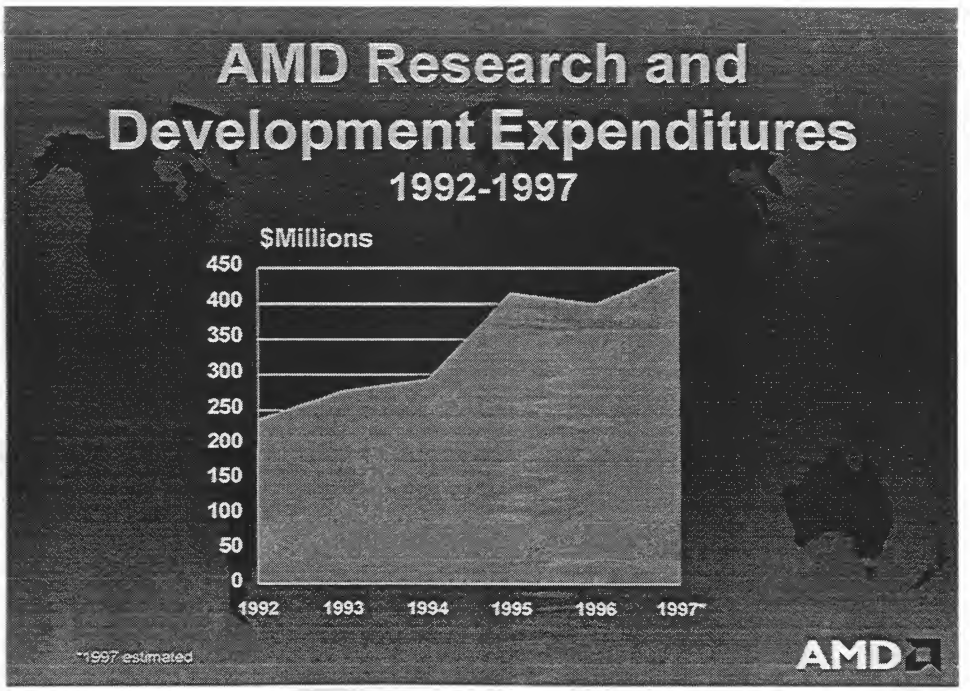
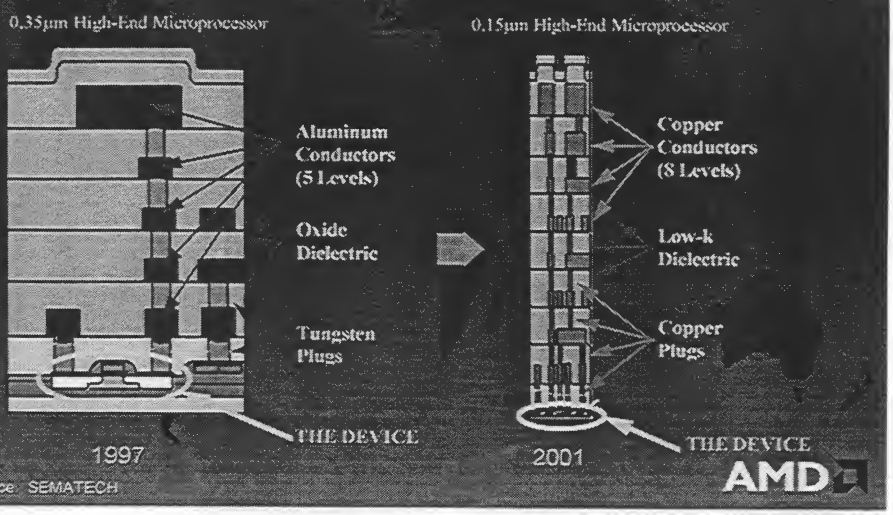

AMD Research and Development Expenditures
1992-1997
$Millions
450
400
350
300
250
200
150
100
50
0
1992
1993
1994
1995
1996
1997*
*1997 estimated
AMD

SEMATECH Processor Technology Roadmap

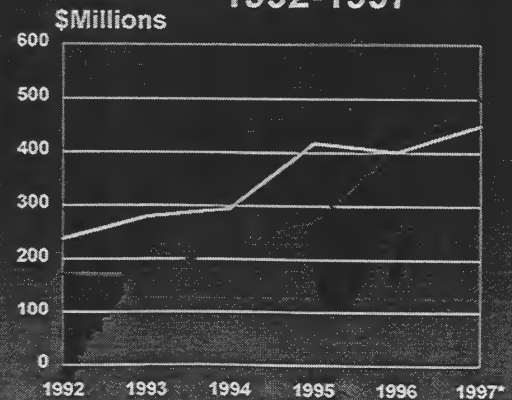


Source: SEMATECH

AMD

AMD and Compaq Research and Development Expenditures

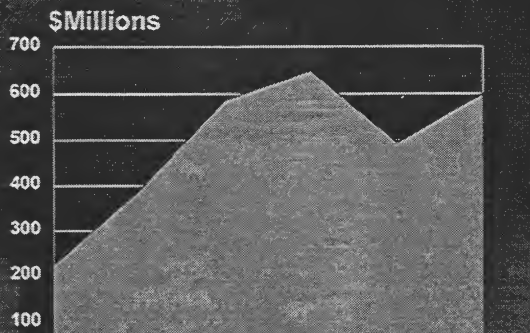
1992-1997



*1997 estimated

AMD

AMD Capital Expenditures
1992-1997



*1997 estimated

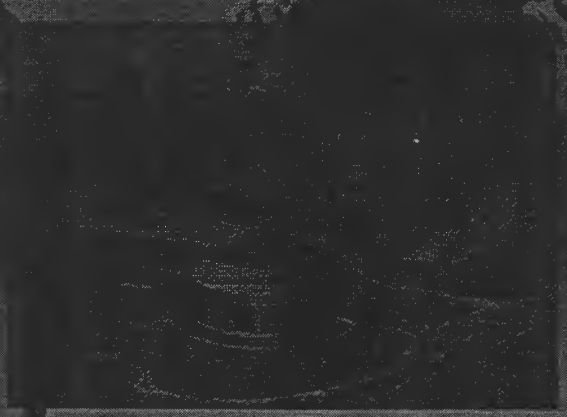
AMD

Submicron Development Center
Sunnyvale, CA

46,000 square feet of cleanroom
Class 1

AMD

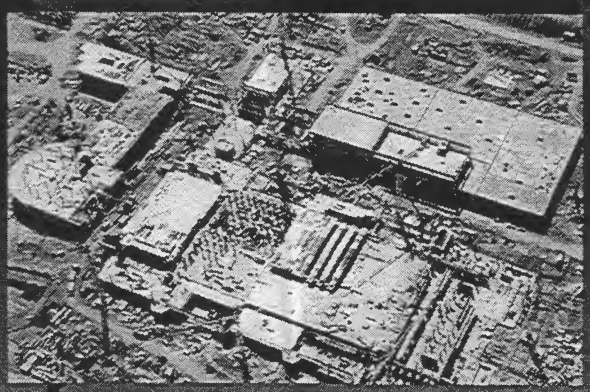
Fab 25
Austin, TX



106,000 square feet of cleanroom
Class 1

AMD

Fab 30
Dresden, Germany



103,000 square feet of cleanroom
Class <1

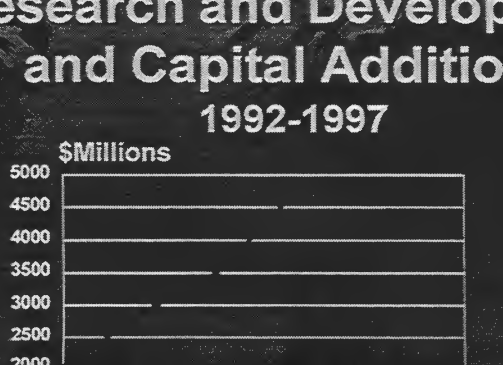
AMD

AMD Expenditures for R&D and Capital
1992-1997

*1997 estimate

AMD

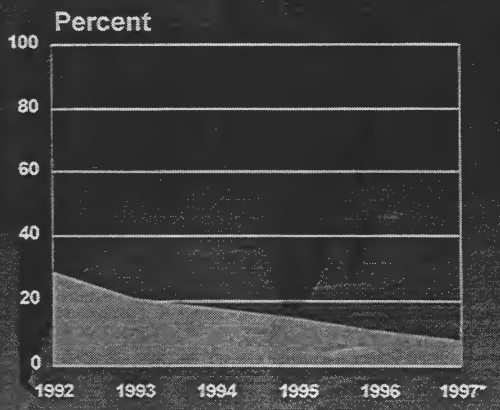
AMD and Intel Expenditures for Research and Development and Capital Additions
1992-1997



*1997 estimated

AMD

AMD x86 Microprocessor Unit Market Share
1992-1997

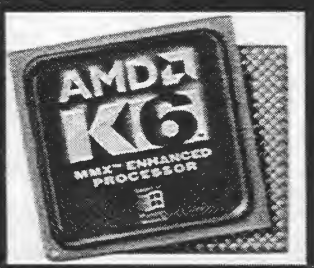


*1997 estimated

AMD

AMD

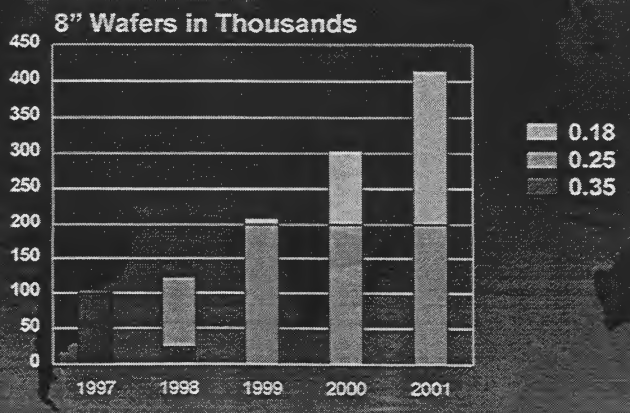
AMD-K6™ MMX™ Enhanced Processor



Microprocessors for the Masses

AMD

AMD Microprocessor Production Capacity by Technology



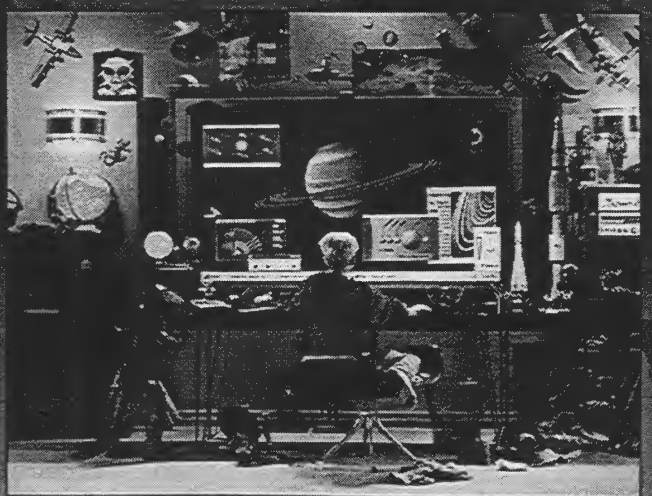
AMD

"And the platform will continue to evolve from the connected PC of the mid-90s to the visual computing platform of the late-90s"

Andrew S. Grove
Chief Executive Officer
Intel Corporation
Remarks at Comdex 1996

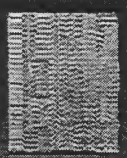
AMD

AMD Leads the Way to the Visual Computing Platform of the Future



AMD

AMD-K6 Family Roadmap



AMD-K6™ MMX™ Enhanced Processor
0.35-micron process
162 mm² die size
8.8 M transistors
233 MHz
1H97

AMD

Socket 7 Q397

AMD K6/233

Frontside Level 2 Cache

66MHz Socket7 Interface

Main Memory

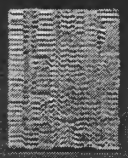
66 MHz

NorthBridge

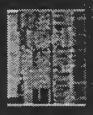
33MHz PCI

AMD

AMD-K6 Family Roadmap



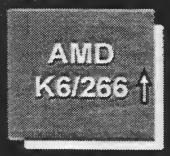
AMD-K6™ MMX™ Enhanced Processor
0.35-micron process
162 mm² die size
8.8 M transistors
233 MHz
1H97

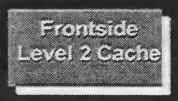


AMD-K6 MMX Enhanced Processor
0.25-micron process
68 mm² die size
8.8 M transistors
266 MHz
2H97

AMD

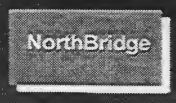
Super7 Phase 1 Q497





66 MHz Socket7 Interface

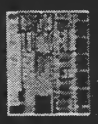
66 MHz



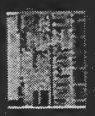
133MHz AGP

AMD

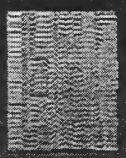
AMD-K6 Family Roadmap



AMD-K6 3D Processor
0.25-micron process
81 mm² die size
9.3 M transistors
300 → 350 MHz
1H98



AMD-K6 MMX Enhanced Processor
0.25-micron process
68 mm² die size
8.8 M transistors
266 MHz
2H97



AMD-K6™ MMX™ Enhanced Processor
0.35-micron process
162 mm² die size
8.8 M transistors
233 MHz
1H97

AMD

Super7 Phase 2 1H98

AMD
K6 3D
300 → 350 MHz

Frontside
Level 2 Cache

100MHz Socket7 Interface

Main
Memory

100MHz

NorthBridge

133MHz AGP

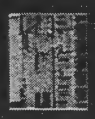
Video
Graphics

33MHz PCI

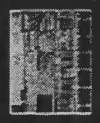
AMD

AMD-K6 Family Roadmap

AMD-K6™ MMX™ Enhanced Processor
0.35-micron process
162 mm² die size
8.8 M transistors
233 MHz
1H97



AMD-K6 MMX Enhanced Processor
0.25-micronprocess
68 mm² die size
8.8 M transistors
266 MHz
2H97



AMD-K6 3D Processor
0.25-micron process
81 mm² die size
9.3 M transistors
300 › 350 MHz
1H98

AMD-K6+ 3D Processor
0.25-micron process
135 mm² die size
21.3 M transistors
350 › 400 MHz
2H98

AMD

Super7 Phase 3 2H98

AMD K6+ 3D 350 → 400 MHz

Full Speed Backside

On-chip Level 2 Cache 256K Bytes

Frontside Level 3 Cache

100MHz Socket7 Interface

Main Memory

100MHz

NorthBridge

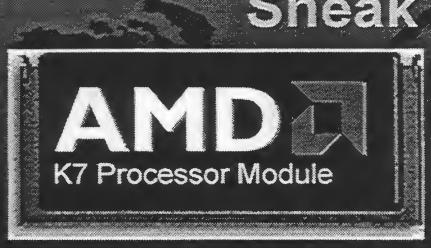
133MHz AGP

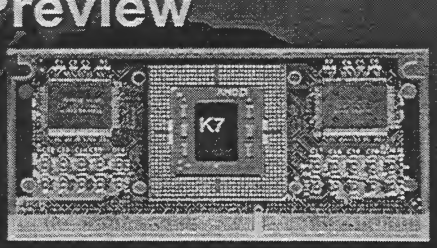
Video Graphics

33MHz PCI

AMD

AMD-K7™ Processor Sneak Preview





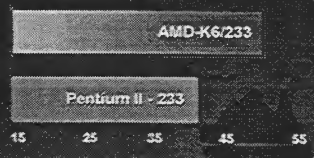
- Driven by customer requirements
- Clock speeds in excess of 500 MHz
- Advanced bus interface, "Alpha" EV6 bus protocol
- Plan of record: slot "A" mechanically identical to Intel's slot 1
- Enabling alternative platforms for 1999 and Beyond

AMD

AMD-K6 Processor is the Smart Choice

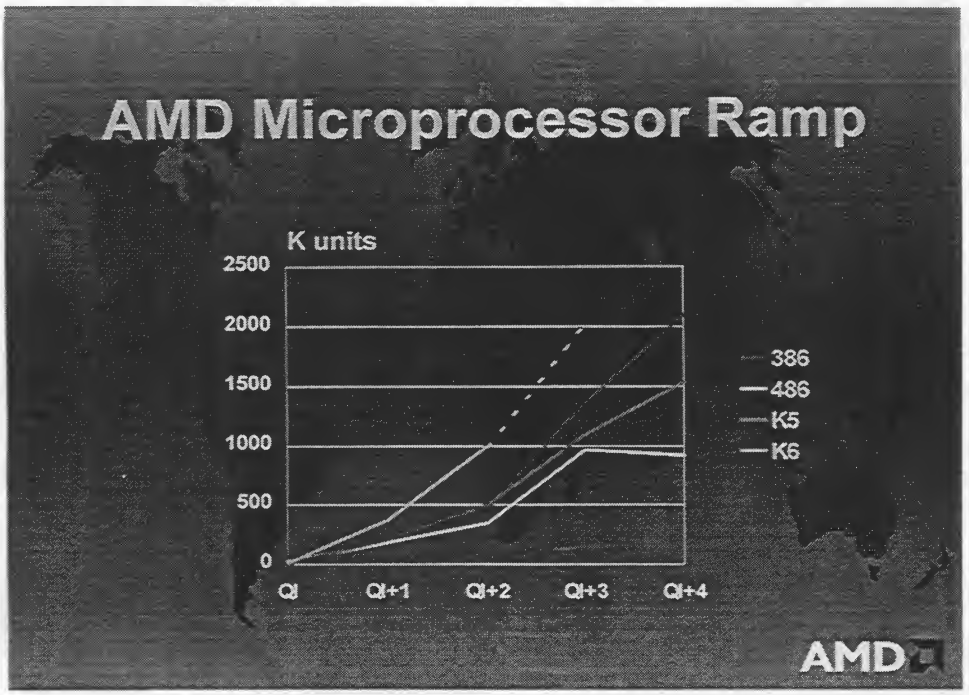
- Much Faster Performance
- More Compelling Features

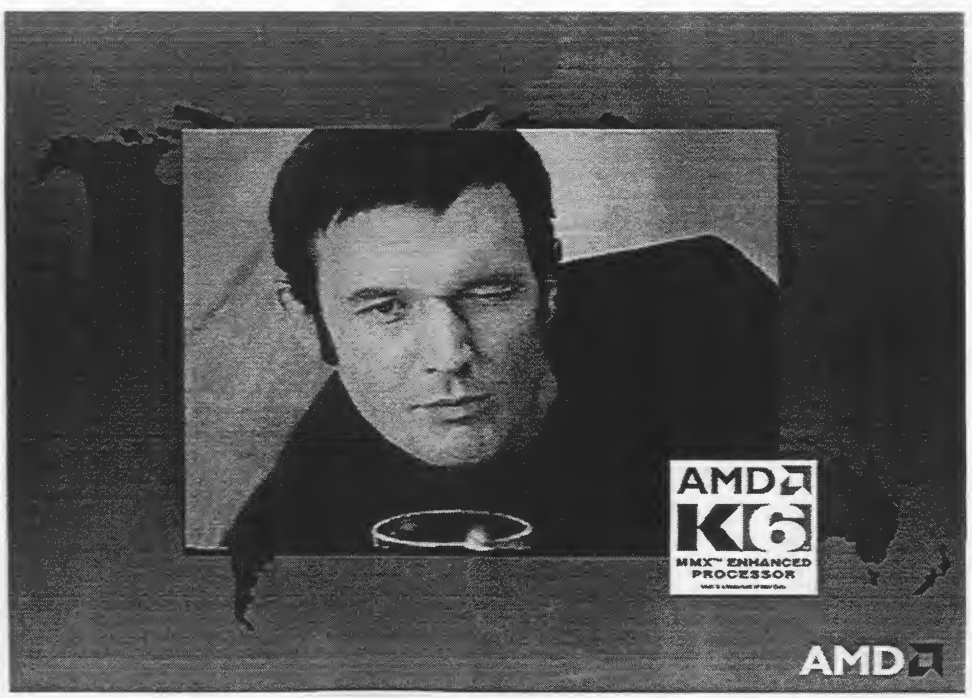
AMD-K6™/233 MMX™ Enhanced Processor	*Pentium® II 233 Processor w/ MMX Technology*	
• 2.5GB Hard Drive	• 2.5GB Hard Drive	*$1,699*
• 32MB SDRAM	• 16MB EDO-DRAM	
• High Performance 4MB Video Card	• High Performance 2MB Video Card	
• 32x CD-ROM	• 16x CD-ROM	
• 56K Fax/Modem	• 33.6 Fax Modem	
• Sound Blaster® AWE64™	• 16-Bit Audio	
• Windows 95 + S/W Bundle	• Windows 95 + S/W Bundle	

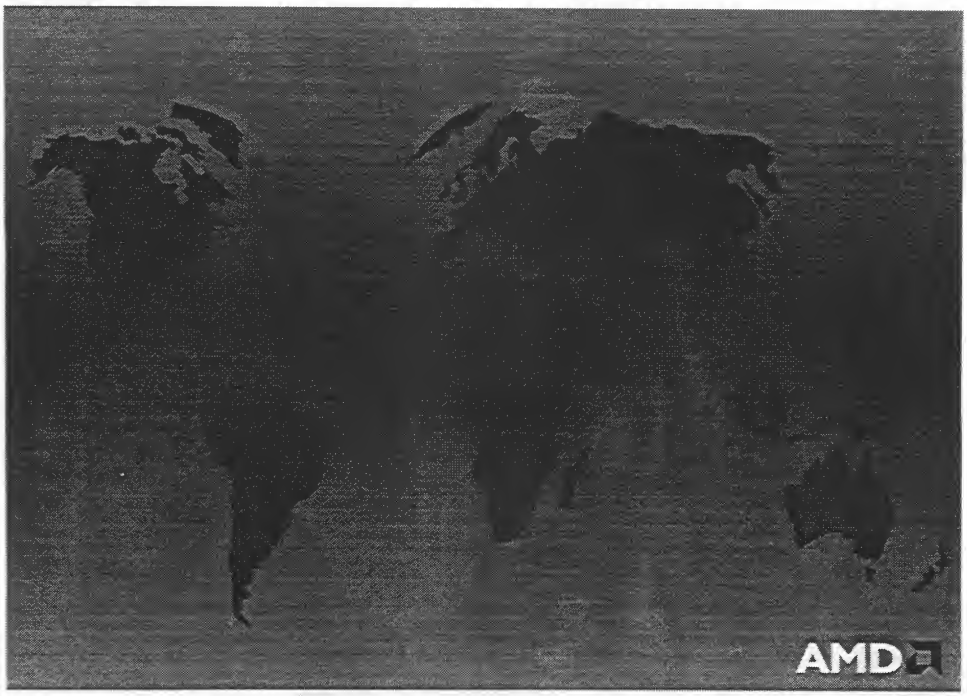


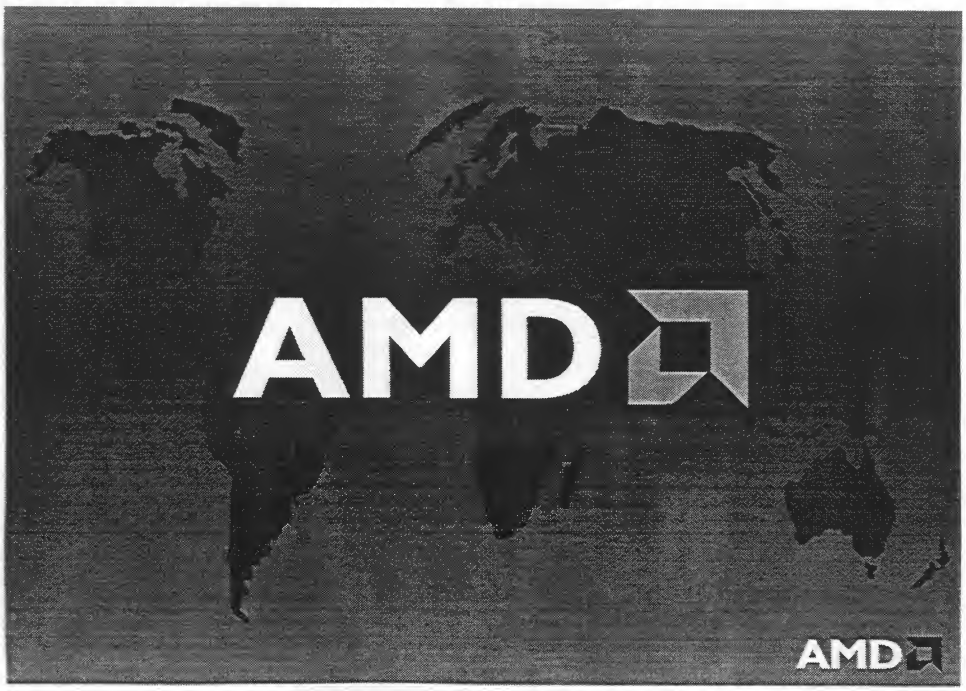
System prices based on Q397 component costs, based on Mercury Research "Desktop PC Build Costs '97 - 2001"
Price estimates based on Computer Retail Week report, 7/17/97 (pcbweb.cmp.com)

AMD


AMD Microprocessor Ramp
K units
2500
2000
1500
1000
500
0
Qi
Qi+1
Qi+2
Qi+3
Qi+4
386
486
K5
K6
AMD


AMD
K6
MMX™ ENHANCED
PROCESSOR
AMD


AMD


AMD
AMD

AMD

AMD-K6™ MMX™ Enhanced Processor Product Roadmap

Agenda

AMD

- **AMD Super7 Platform Initiative**
  - Advancing the Socket 7 Platform
- **AMD-K6™ Product Roadmap**
  - AMD-K6 3D
  - AMD-K6+ 3D
- **AMD-3D™ Technology**
  - 3D Multimedia Instruction Set

Super7: Socket 7 Enhancement Initiative

- **Key Performance Enhancements**
  - Addition of AGP in '97
  - Higher local bus frequency - 100 MHz
  - Support for 100 MHz frontside cache
  - Maintains socket 7 compatibility and cost advantages
- **At Leading Edge of all System Feature Advancements**
  - Today: USB, SDRAM, UDMA, ACPI
  - Future: AGP, PC 98, 100 MHz bus, 100 MHz SDRAM, 1394, etc
- **System Logic Vendors: ALi, National, SiS, VIA and AMD**

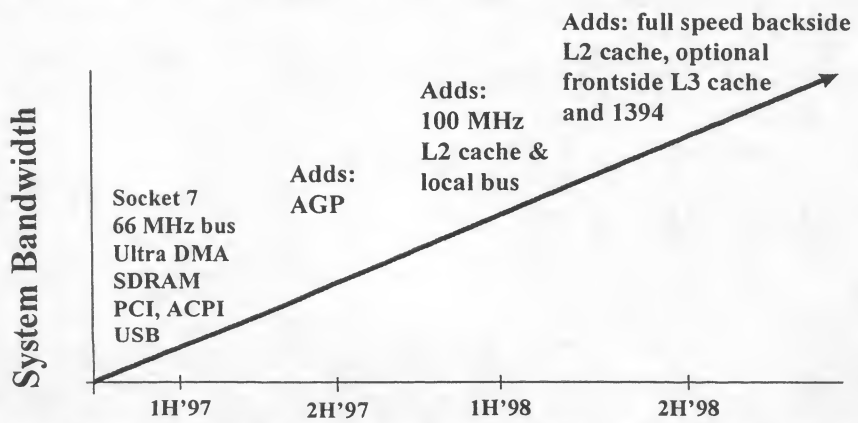
AMD is committed to leading the socket 7 infrastructure to higher performance!

AMD @ work — AMD-K6™ MMX™ Enhanced Processor — Microprocessor Forum '97

3

AMD-K6 Super7 Roadmap

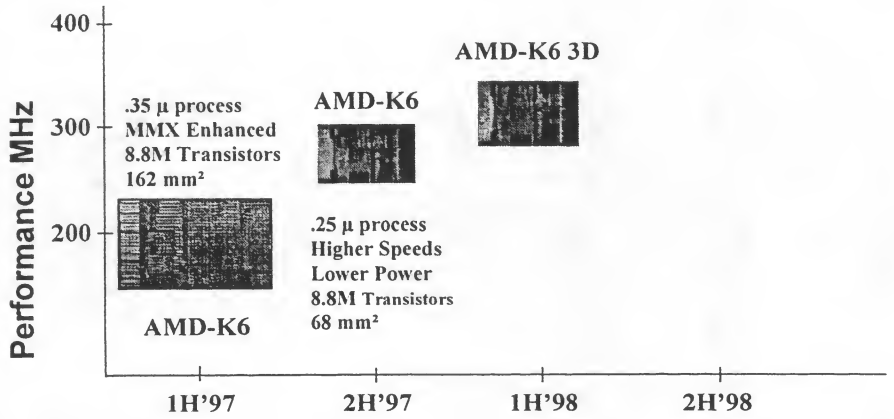
"For a uniprocessor system, the Pentium® bus is just as good as - if not better than - the P6 bus."!
Michael Slater, Microprocessor Report Dec 30, 1996



AMD @ work — AMD-K6™ MMX™ Enhanced Processor — Microprocessor Forum '97

4

AMD-K6 Processor Family Roadmap



AMD @ work — AMD-K6™ MMX™ Enhanced Processor — Microprocessor Forum '97

5

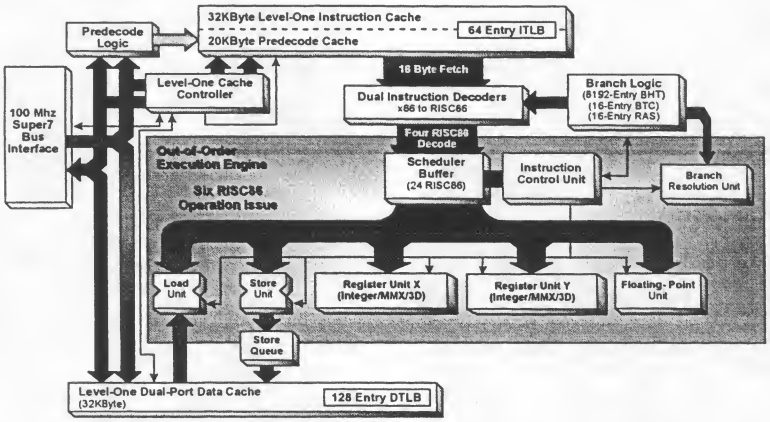
AMD-K6 3D™ New Processor Features

- **AMD-3D Technology**
  - Instruction set extensions to accelerate 3D graphics, audio and other multimedia applications
- **Superscalar MMX Units**
  - Dual decode and dual execution pipelines
  - Maintains the K6 advantage of low execution latencies
  - No decode pairing restrictions
  - Only one cycle misalignment penalty on memory accesses
- **100MHz Local Bus**
  - Increases local bus and L2 cache bandwidth by 50%
  - Redesigned I/O timing to allow for low cost 100 MHz motherboard
- **9.3 Million Transistors on a Die of 81mm²**

AMD @ work — AMD-K6™ MMX™ Enhanced Processor — Microprocessor Forum '97

6

AMD-K6 3D Block Diagram



Acceleration of Multimedia Applications

- **Multimedia applications have grown to become an integral part of the PC platform**
  - But multimedia algorithms are very computation intensive

Application or Game Physics	Geometry transform, Clipping, & Lighting	Triangle Set up	Pixel Rendering
			
floating point intensive	floating point intensive	floating point & integer intensive	integer intensive

  - MMX extensions where added to accelerate integer multimedia algorithms, but the impact on the user experience has been limited since MMX accelerated only some computations.

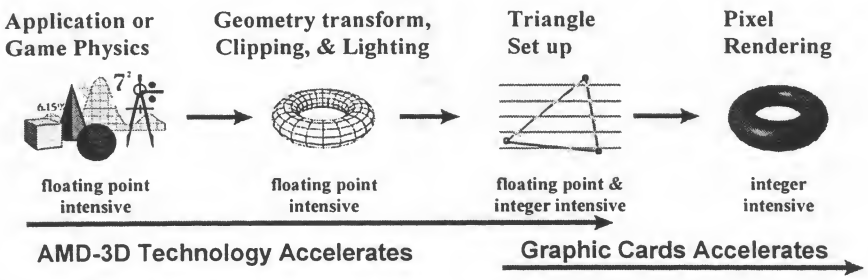
AMD-3D Technology

AMD

- **Why a New Technology?**
  - Generally only graphics pixel rendering has been accelerated by MMX and 3D graphics hardware; focus has been on integer performance
  - 3D graphics performance is now limited by the earlier floating point intensive stages of the graphics processing pipeline
  - Realistic physical modeling is also becoming a necessity
- **What is it?**
  - A new set of instructions to greatly accelerate floating point computations
  - Multiple floating point operations per clock
  - Defined and implemented in collaboration with leading ISV's
  - Works in concert with graphics accelerator cards by speeding up the front end of the graphics pipeline

AMD-3D Technology

AMD



- **Benefits**
  - Relieves the floating point intensive bottlenecks in 3D graphics processing
  - Allows for more detailed physics-based modeling and simulations - more objects with accurate physical characteristics displayed at life-like speeds.
  - Accelerates most floating point intensive multimedia operations:
    - Graphics pipeline (Physics, Geometry, & Set up)
    - Audio processing (AC-3 and 3D)

AMD-3D Technology

AMD

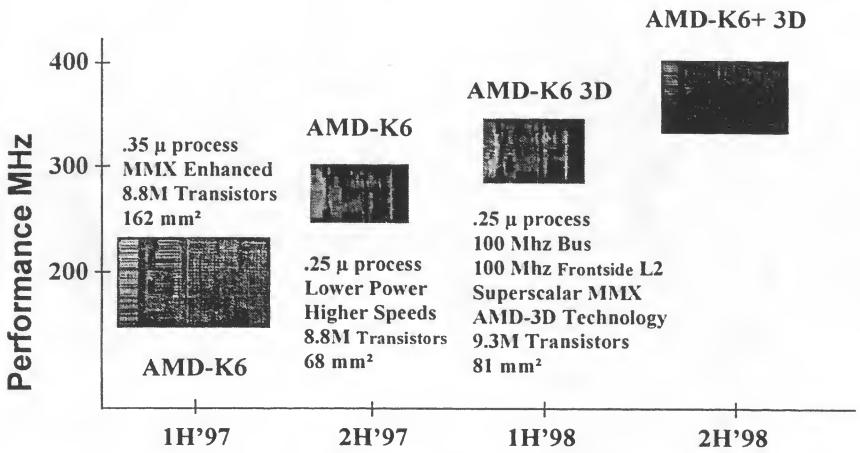
- **SIMD Floating Point Instructions**
  - Supports IEEE Single Precision Data Type
  - Two 32-bit FP values per 64-bit reg/mem operand
  - Uses MMX Registers
- **24 New Instructions**
  - PFMUL, PFADD, PFSUB, PFCMP, PF2I, PI2F,etc.
  - Similar encoding format to MMX Instructions
- **Streamlined for High Performance**
  - Saturating arithmetic
  - No exceptions
  - Limited rounding modes
  - No switching overhead between MMX and AMD-3D instructions
  - Avoids X87 register stack

AMD-3D Technology: Software Support

AMD

- **Enthusiastic Support from Major ISV's**
- **Full Software Development Support**
  - Full Microsoft Support
    - Assembly language - native Microsoft MASM support
    - Fully optimized API and libraries at introduction: DirectX (Direct3D & DirectSound) and OpenGL
  - Profiler and optimizer tools
  - AMD SDK available to AMD NDA partners
- **Dedicated AMD Development Support Group**
- **No Core OS Support Required**

AMD-K6™ Processor Family Roadmap

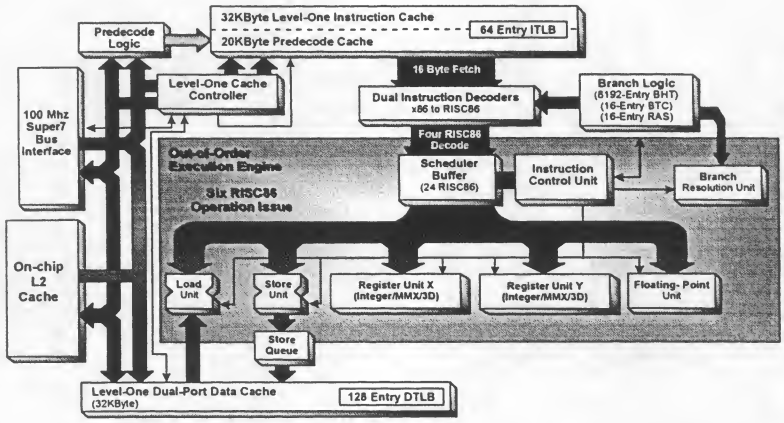


AMD-K6+ 3D Processor Features

- **On Chip Full-speed Backside Level 2 Cache**
  - Operates at 1X processor frequency
  - 4-1-1-1 (-1-1-1-1) access timing (Peak Bandwidth 3.2 GB/sec at 400 MHz)
  - 256K byte
  - 2-way set associative
  - In addition to current 64 KB L1 cache
- **Improved Write Buffering, Pipelining, and Combining**
- **Large Level 2 TLB - Higher Performance Paging**
- **Maintains Full Socket 7 Compatibility**
  - 100 MHz frontside local bus
  - Optional very large frontside level 3 cache
- **21.3 Million Transistors on a Die of 135 mm²**

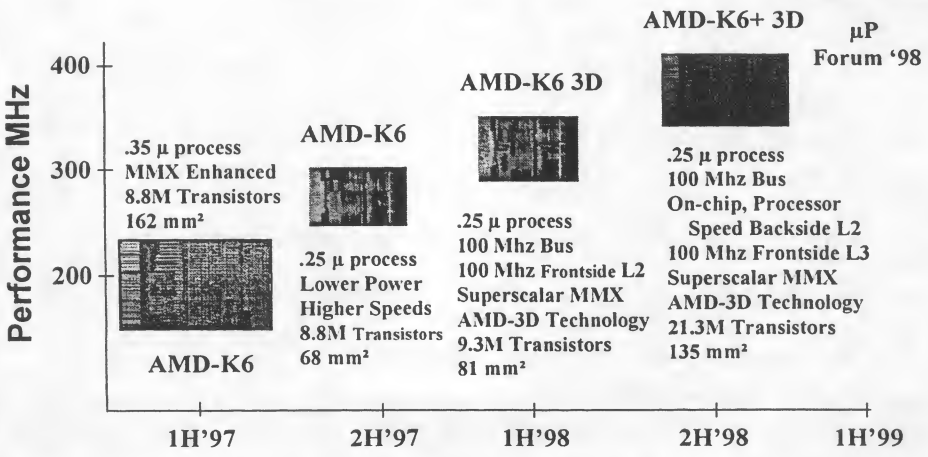
AMD-K6+ 3D Block Diagram

AMD



AMD-K6™ Processor Family Roadmap

K7



Summary

AMD

- **Super7: 100 MHz frontside bus with AGP**
  - Leading edge platform initiative that achieves Socket 7 architectural performance improvements
- **Robust AMD-K6 Product Roadmap for '98**
  - Major CPU architectural performance improvements
  - Higher frequencies
  - 100% compatibility with Socket 7/Super7 infrastructure
  - On-chip level 2 cache
- **AMD-3D Technology:**
  - New instruction set of extensions that greatly accelerate 3D graphics, audio and other floating point intensive multimedia algorithms
- **AMD, Enabling a Higher Level of Application Realism.**

Evolution of IA-32 System Design

Bob Colwell

Intel Fellow

Director IA-32 Architecture

intel.

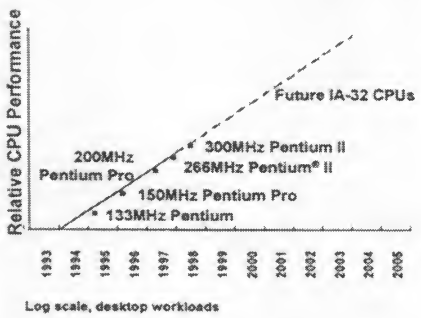
Market Forces Driving Design Changes

- Exploding demand for high-performance mid-range and above servers and workstations based on standard platforms
  - CPU performance continues skyrocketing
  - L2 caches getting bigger at similar pace
  - Multiprocessing now needed and feasible
- Large market segments justify differentiation
  - "Purpose-built" processor products
  - Platform specific product form factors following segments

P6 core designed to serve multiple market segments with products differentiated at platform level

intel.

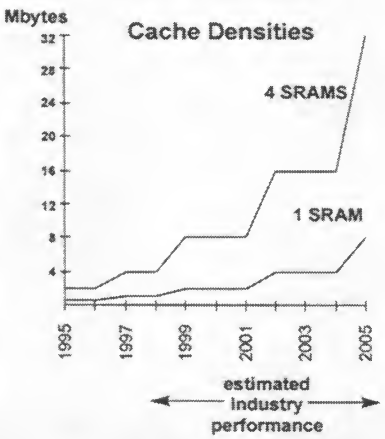
CPU Trends



- Deschutes: next IA-32 CPU
  - P6 at 333+ MHz in 1998
- Moore's Law performance spiral continues
- Big caches and multiprocessing now standard in high end market segments
- Faster microarchitectures make more demands on cache & memory

intel.

Industry Cache Trends



- Cache sizes double for each new process
- Can combine multiple SRAMs for large caches
  - If product engineered for it!
- Performance scaling not linear with size
  - Latencies not improving as fast as capacity
  - Still, larger means higher system performance on server workloads

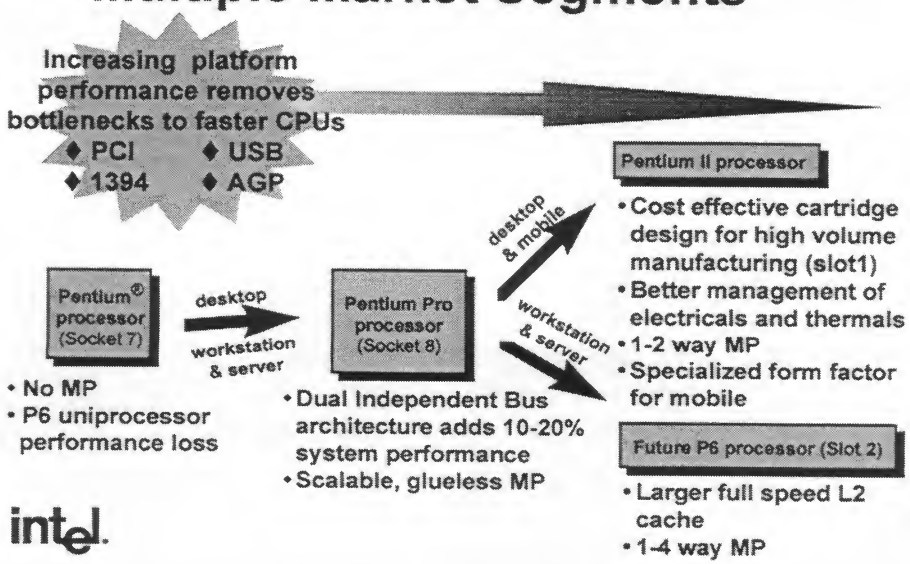
intel. *Must build in headroom for future caches*

Design Problem: System Bottlenecks

- New features, faster CPUs require faster rest-of-system (else bottlenecks arise)
  - MP, PCI, 1394, USB, hi-res graphics, real-time video
- Backside L2 caches, bigger sizes, latencies, fast pipelining
- Larger main memories
- Need faster system buses
  - Especially with stream-oriented workloads
  - Good solution for Pentium® processor system bus (socket 7)
  - But unsuited for multiprocessor workstations & servers

intel.

Design Problem: One CPU, Multiple Market Segments



intel.

Design Response: Slot 1

- High performance at volume price points
  - Still want/need performance boost from fast nearby L2 cache
  - Cartridge manufacturable at very large volumes
  - Cartridge permits close control of electricals and thermals
- Commodity SRAMs help economics
  - Vs. Pentium® Pro processor's custom SRAMs
- Desktop DP-only implies smaller caches ok
  - Cartridge fixed in size, thermals, power supply to control cost

The Pentium® II processor Slot 1 cartridge was created to get P6 microarchitecture to volume markets

intel.

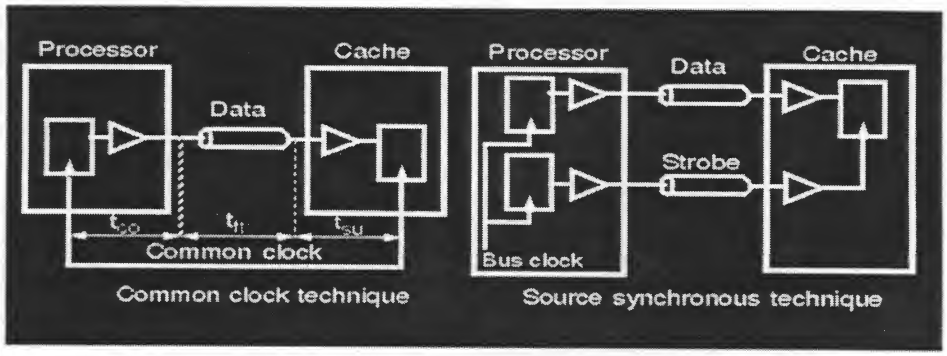
Design Response: Slot 2

- Large market segments emerged above desktop
  - Require highest performance, higher cost ok
  - Can handle larger cartridges, thermals, power supply
- 4 way multiprocessing needs bigger caches, higher system bus bandwidth
  - Custom SRAMs ok economically
- Full speed caches need careful cartridge electricals
  - Manage longer latencies with latency hints, upstream caches, streaming buffers, compilers...
  - Beyond 200MHz: Source Synchronous signaling

Slot 2 does not replace Slot 1, it complements Slot 1

intel.

Design Response: Source Synchronous Signalling



- Clock at L2 tracks data transmission delays

intel.

Deschutes: a 0.25μm P6 Core CPU

	Slot 1	Slot 2
L2 Cache	Half speed 512KB	Full speed >512KB
System bus	66 MHz system bus (1H98) 100 MHz system bus (1H98)	100MHz system bus (mid'98)
Clock rates	333MHz core > 333MHz core	> 333MHz core
Availability	1H98 Mobile 1H 98	Mid-98

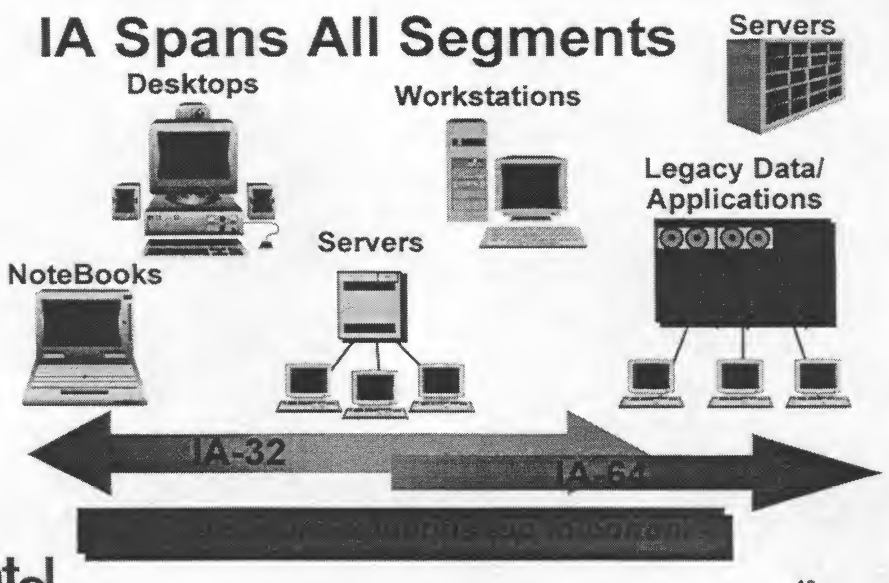
intel.

Conclusions

- P6 microarchitecture enables specialized products for each market segment
  - One CPU core, multiple cache/bus solutions
  - Complementary two-slot strategy balances design requirements of fast cache buses with market-specific cost constraints
- Strategy: Compelling processor products to all market segments
  - Intel IA-32 continues focus on all but highest end segments

intel.

IA Spans All Segments



intel.

12

IDT WinChip C6+: The Next Generation

WinChip Background

- Started 4/95 (4 in my kitchen, home PC, etc)
- Designed IDT-C6 Processor (Ann'd 5/97)
  - P55-compatible (Includes MMX™)
  - Optimized for business applications
  - Smallest 0.35µ die (88 mm^2) ➔ lowest cost
  - 8.9 W max power at 200 MHz (3.3V)
- Started Production Shipments In Sept
  - Windows certified, XXCAL Platinum certified
  - 4 BIOSes available, 10's qualified boards
  - Targeting tier 3 sub-$1000 PCs
  - Primarily via distribution (HHT, Wyle)
- 180 ($90) & 200 MHz ($135) Shipping Now
  - 225 & 240 Sample In November

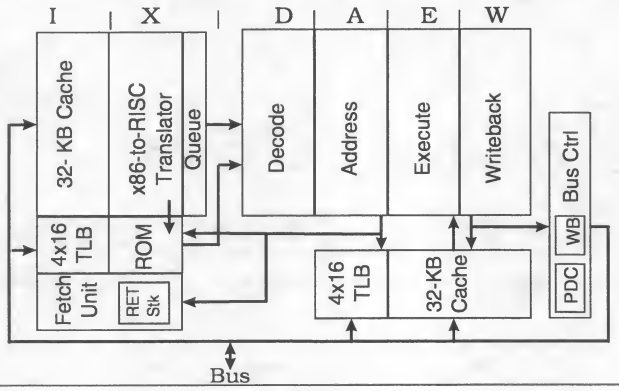
Designed for Microsoft Windows 95

MMX is a trademark of Intel Corporation

2

IDT C6 Architecture

- Simple RISC Pipeline
  - Highly tuned for high MHz & small size
  - Large caches (64 KB), large TLBs, etc.
  - Many non-obvious tricks for x86 (50 patents filed)



3

Next Generation Goals (C6+™)

- "2x" MMX & FP CPI Improvement
  - For those who care (not everyone)
  - Primary FP focus is 3D graphics
- Some Winstone CPI Improvement
  - Already very competitive
- Same Small Die Size (at same 0.35µ)
  - Exploit our small-size design & methodology
- Support New Technologies
  - 2.5V transistor & 0.25µ shrink
  - Faster MHz, lower cost, less power
- Ship 6 Months After C6
  - Exploit our fast development cycle

4

IDT C6+ MMX Improvements

- Full MMX Pairing (Superscalar)
  - Dual MMX units ala P55 (1 multiplier, 1 shifter)
  - 2 Instructions decoded, issued & executed per clock
  - Same pairing rules as P55
- Faster MMX Instruction Timing Than P55
  - 1 cycle multiply latency (vs 3) !
  - 1 cycle multiply-add latency (vs 3) !
  - 1 cycle store (vs 2)
- No MMX-Integer Pairing
  - But, larger caches, larger TLBs, etc.
- Result: Better MMX Performance Than P55
  - *Even on biased Intel Media Benchmark!*

5

IDT C6+ FP Improvements

- Fully Pipelined (Complete Redesign → Same Size)
- Some Instructions Slower Than P55
  - FMUL → 4/2 or 3/1 (SP) (vs 3/1)
  - FXCHG → 1 (vs 1/0)
  - 1 clock penalty on register-memory forms
- Some Instructions Faster Than P55
  - FST → 1 (vs 2-3), FIST, FSTSWAX-SAHF, etc.
- Results: 80-100% P55 FP Performance
  - 80% on biased Intel Media Benchmark (FP)
  - Typically same/faster P55 on real FP applications
- We Intentionally Stopped Here!
  - Silicon better spent on 3D assists/Winstone/etc.

6

3D Graphics Improvements

- 53 New x86 Instructions (12 x86 opcodes)
  - Designed to speed coord transforms/lighting
  - Addresses 20-50% CPU time in heavy-duty 3D
- 22 Additional FP Registers
- Minimal Die Size Impact (< 1mm^2)
  - Primarily reuse of existing dataflow
  - New instruction decodes, a few muxes, etc.
- Intended For Distribution In Future MS D3D
  - Working with Microsoft to add our code
  - Automatically selected machine-specific code
  - Transparent to applications & users

7

3D Graphics Improvements

- Base Instruction Functions (Hdw)
  - 22 additional FP registers (30 total)
  - 1-clock multiply-accumulate
  - 1-clock load of 2 single-precision (SP) values
  - 1-clock compare & set bit flags
  - Fast SP inverse square root, square root, divide
  - 1-clock convert to/from integer
  - Fast & flexible moves to/from integer registers
  - Individual instruction control of precision
- Microcode Instructions For Future Speedups
  - Multiple clocks initially → single clock in future
  - 2x & 4x multiply-accumulates
  - Store 2 single-precision values at once

8

3D Graphics Improvements

Results (SP data)	*Best P55* [1]	*C6+* [2]
■ [x y z] Transform (12 values)	34	14 clks
■ 1/sqrt($x^2+y^2+z^2$)	125 (hw) ≈80 (sw)	29
■ [x y z] Edge Detect (6)	37	8
Total	196	51
■ etc.		

Notes

1. Highly optimized low-level assembler code for P55. Much better than any real code that we have found in programs/benchmarks.

2. Highly optimized low-level assembler code for IDT C6+.

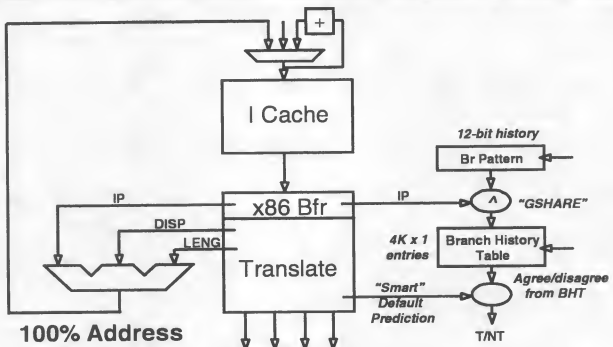
9

IDT C6+ Integer Improvements

- Many Misc Improvements
  - Multiply ➔ 6 (vs 10 for P55)
  - Load-ALU-Store ➔ 2 (vs 3 for P55)
  - No penalty for 0F prefixes
  - Reduced AGIs, no penalty on base+index, etc.
- Limited Instruction Pairing
  - PUSH-PUSH, POP-POP
  - Pairs executed in same clock
- Generate Up to 4 Micro Instructions per Clock
  - Helps fill queue faster ➔ key to branch prediction
- Great Branch Prediction
  - Better performance & much smaller than P55

10

IDT C6+ Branch Prediction



100% Address Prediction on 99% of Branches

Predicted Taken
- 2 clks if Q empty
- else 1 clk (85%)
Predicted Not Taken
- 1 clock

Highly Accurate "Two Level" Prediction

11

IDT C6+ Branch Prediction

	P55	*C6*
BTB/BHT Bits	34 Kb	4 Kb
Correctly Predicted Branch	1	1-2 clks (1.1 avg)
Mispredict Time	5-6	4 clks
Predict Rates		
- Norton SI32	77%	89%
- Winstone Business	82%	93%
Avg Branch Clocks		
- Norton SI32	2.03	1.41
- Winstone Business	1.81	1.30

12

System Perf Improvements

- 4-way D-Cache (vs. current 2-way)
- Write Allocate (optional)
- Weak Read Ordering (optional)
- Plus Branch Prediction, etc.

Results

- 6% Faster Winstone 97 Business (Win95)
  - As fast as anyone at same MHz (P55, K6, M2)

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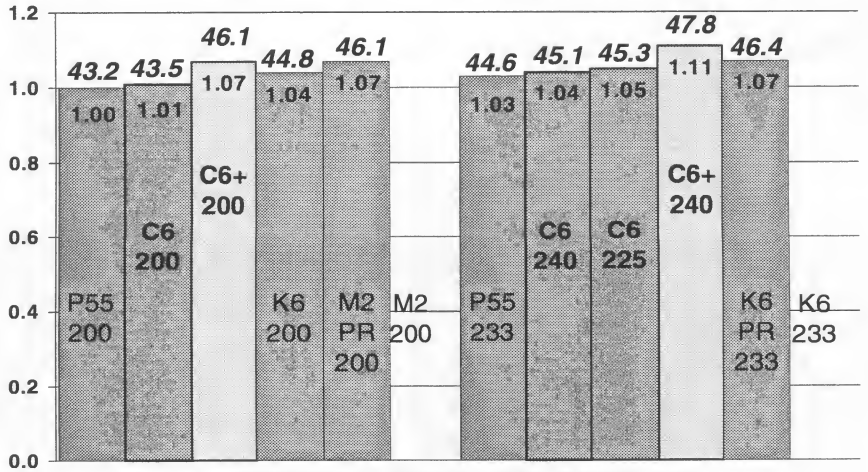
Business Performance

Low-end commodity desktop (TX, 512 KB, 32-MB EDO, S3 Virge)



Winstone97 (Business) for Windows 95

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IDT C6+ Summary

- 2x C6 MMX CPI Performance
  - Better Than P55 MMX (on its own benchmark)!
- 2x C6 FP CPI Performance
  - Worst-case 80% of P55 (biased Intel Media BM)
- 2-4x P55 CPI on Specific 3D Graphics Kernels
  - Will be transparently available via MS D3D
- 6% Winstone CPI Improvement
  - As good as any other socket 7 at same MHz
- Support For New Technology (Split Voltage)
- 91 mm^2 vs. 88 for Current C6 (both 0.35μ)

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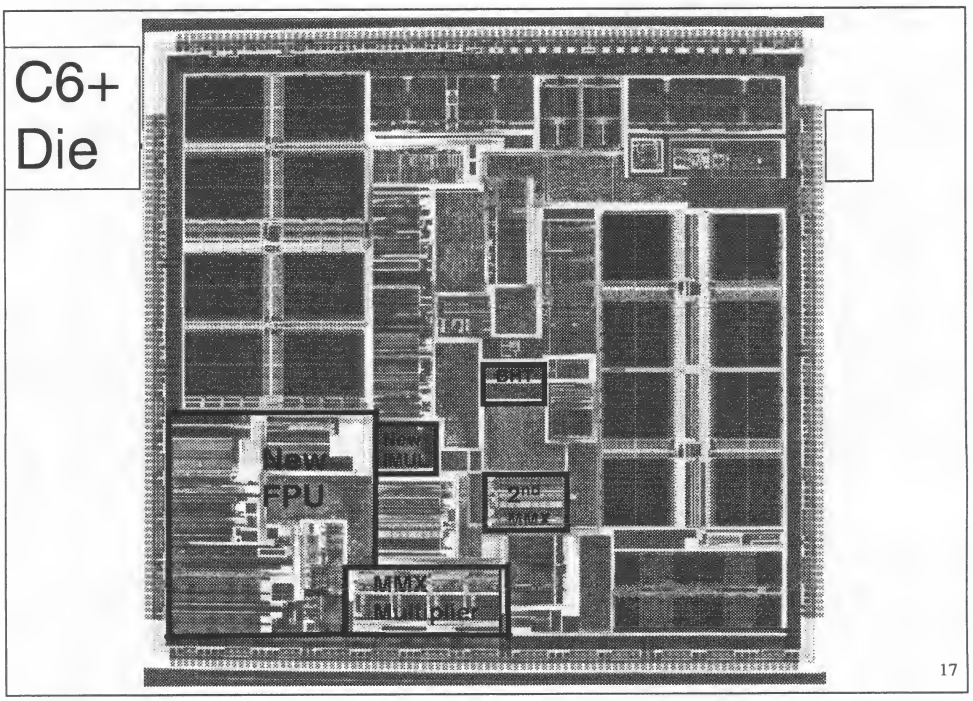
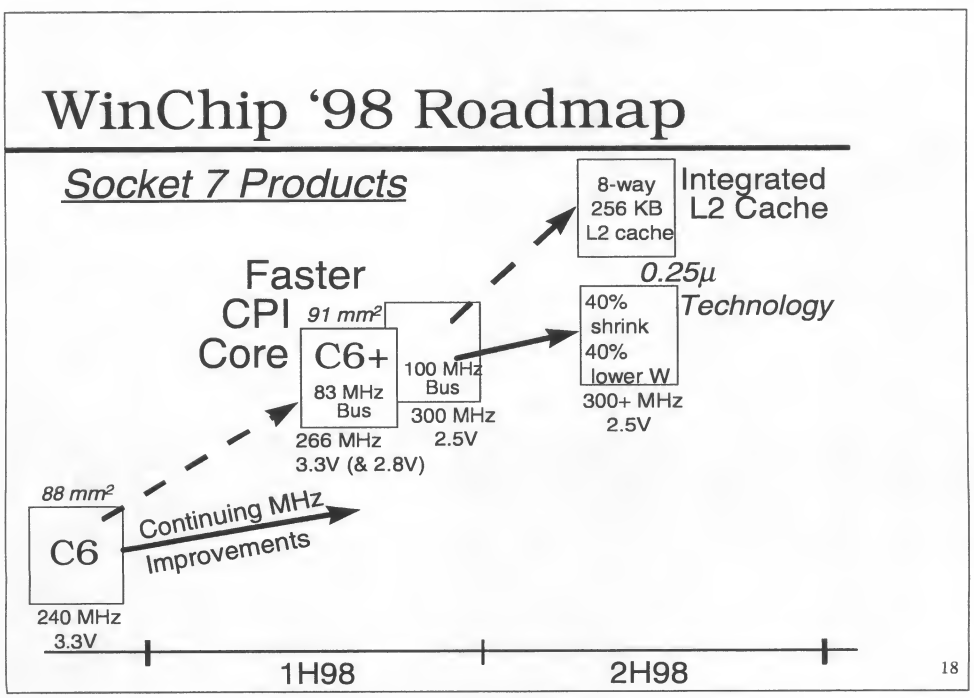
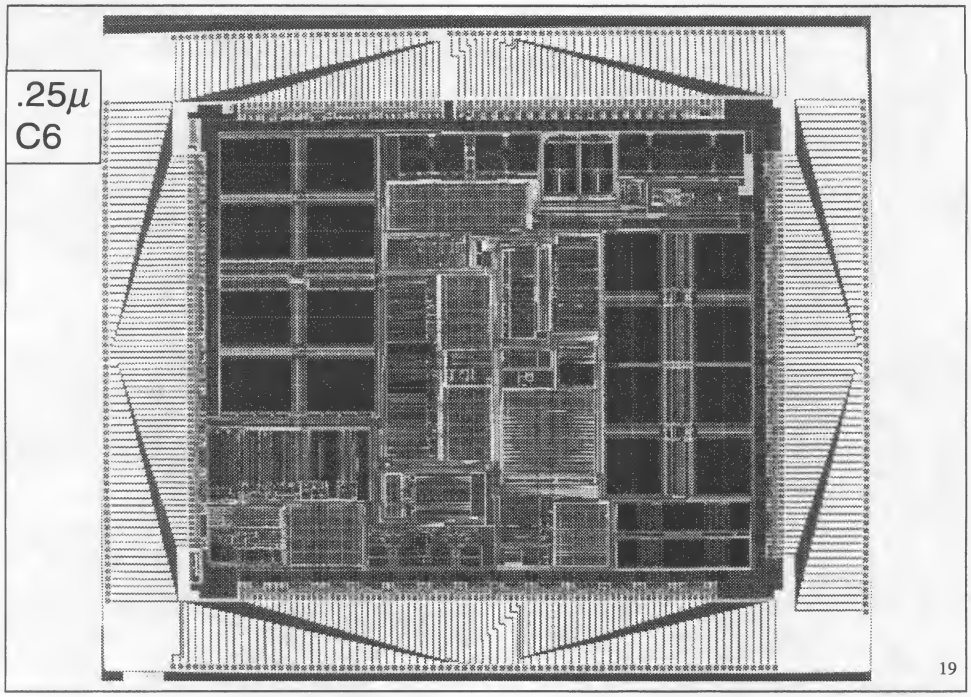
IDT C6+ Summary

- Production Tapeout 11/15
- Target Shipments 2Q98
  - Samples 1Q98
- Two Technology Options
  - 3.3V core
    - Up to 266 MHz
    - Split V core allows reduced power & MHz
  - 2.5V core
    - 300 MHz at first ship
    - 40% lower power (at same MHz)
    - 3 months after 3.3V version

16


C6+
Die
New
FPU
MMX
Multiplier
17


WinChip '98 Roadmap
Socket 7 Products
8-way
256 KB
L2 cache
Integrated
L2 Cache
0.25µ
Technology
Faster
CPI
Core
91 mm²
C6+
83 MHz
Bus
266 MHz
3.3V (& 2.8V)
100 MHz
Bus
300 MHz
2.5V
40%
shrink
40%
lower W
300+ MHz
2.5V
88 mm²
C6
240 MHz
3.3V
Continuing MHz
Improvements
1H98
2H98
18


.25μ
C6
19

Competitive Strategies for x86 Microprocessors

Michael Slater, *MDR*

presented by MICRODESIGN RESOURCES

Competitive Strategies for x86 Microprocessors

Michael Slater
Principal Analyst
MDR

Changes in the Past Year

- Rapid shift to processors with MMX
  - Pentium → Pentium/MMX
  - Pentium Pro → Pentium II
  - K5 → K6
  - 6x86 → 6x86MX
- Intel's Pentium II introduces Slot 1
- 3D generates broad interest in FP
- Cyrix acquired by National
- IDT/Centaur joins the fray

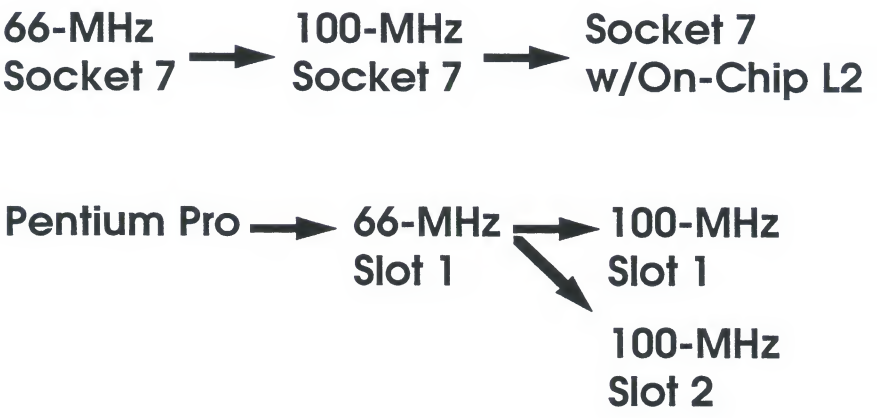
MMX Takes Over

- Rapid shift to MMX processors driven more by other features of those processors than by MMX itself
  - Larger caches, faster clock speeds
- Marketing has convinced users to want MMX, but applications are few
  - MMX has become a standard part of the architecture, making it largely a non-issue

Growth in the Low End

- Fastest growth in low-cost PCs
- Cyrix's MediaGX won role at Compaq by offering price advantage
  - First successful high-integration PC processor
- Intel's focus on higher price points makes this segment an opportunity for Intel's competitors
  - But it is hard to make much money

System Interface Trends



Questions for 1998

- Will Intel's competitors be able to match Intel's FP/MMX performance?
- Will Intel succeed in moving the mainstream market to Slot 1?
- Can Intel's competitors keep Socket 7 performance competitive?
- Will proprietary instruction set extensions succeed?
- Is there a role for integrated processors?

Pentium II Design Enhancements

Robert Colwell, *Intel*

presented by MICRODESIGN RESOURCES

The AMD-K6 Plus: An Enhanced K6 Microprocessor

Greg Favor, *AMD*

presented by MICRODESIGN RESOURCES

A New, High-Performance x86 Microprocessor

Robert Maher, *Cyrix*

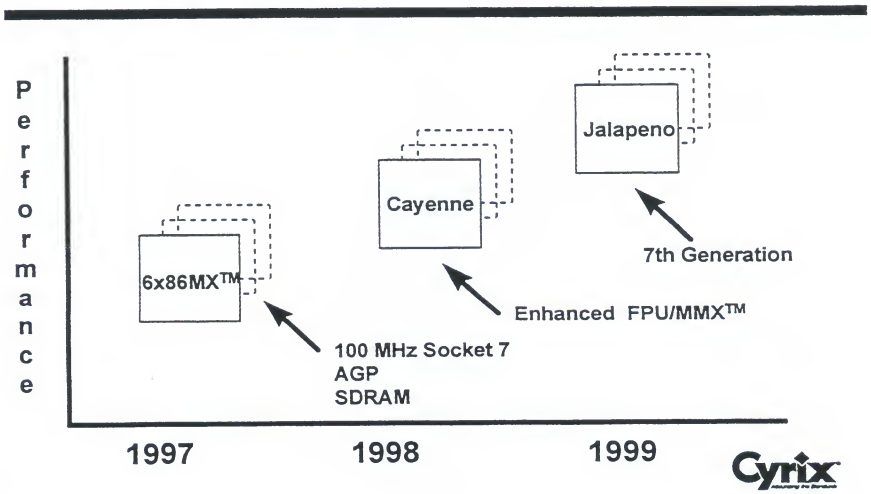
presented by MICRODESIGN RESOURCES

Beyond the 6x86MX™ Processor

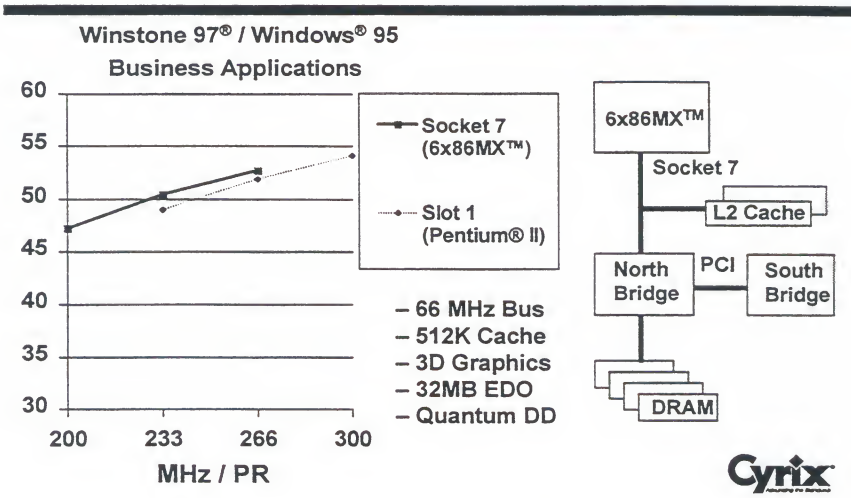
Robert Maher
Vice President of Engineering
Cyrix Corporation

www.cyrix.com

Core Roadmap



Socket 7 Today



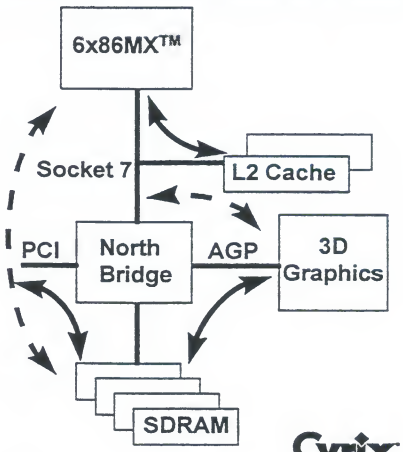
Socket 7: The Future - 6x86MX™

- AGP support in Q1 1998
- 100 MHz system bus Q1 1998
  - Lookaside caches: Up to 2MB support
    - Tag RAM in north bridge
    - 5ns data RAMS
    - 3-1-1-1 line fills
- SDRAM today, DDR SDRAM 2H 1998
- Firewire (IEEE 1394), Device Bay, ATA66

Cyrix

The Socket 7 System

- Balanced system design
  - Concurrency
    - CPU <—> L2
    - PCI <—> MEM
    - AGP <—> MEM
  - Concurrency
    - CPU <—> MEM
    - CPU <—> AGP
- Multimedia applications have data sets > 2MB therefore latency to main memory is critical



Cyrix

Socket 7 System Performance

- As core frequency improves, L2 cache at 100 MHz keeps L1 miss penalty (core clocks) consistent with 66 MHz systems
- 100 MHz system bus ⇨ 50% increase in L2 cache performance
- Low latency / High bandwidth path to main memory
  - 100 MHz Socket 7 bus
  - 100 MHz SDRAM

Performance will scale with 100 MHz system bus

Cyrix

Beyond 6x86MX™: Cayenne Core

- Based on 6x86MX™ core
  - 4MB paging
  - Virtual mode enhancements
  - Frequency optimizations
- 64KByte L1 cache
- Pipelined, dual-issue FPU
- Enhanced MMX technology
- .25 micron process technology

Cyrix

Cayenne Core: FPU

- Dual-issue floating point
  - 2 FOP
  - 1 load / 1 store, 1 FOP
  - Instruction queue
- Fully pipelined floating point unit

Throughput / Latency

	Cayenne	6x86MX
FXCHG	0	2/2
LOAD/STORE	1/4	4/4
ADD	1/4	4/4
MULTIPLY (SP)	1/4	4/4
MULTIPLY (DP)	3/6	6/6

Cyrix

Cayenne Core: MMX

- Dual Issue / Dual Execute
  - 1 shift / 1 multiply
  - 2 MMX add/logical units
  - 1 load / 1 store
- Fully pipelined
- Single-cycle execution
- Multiplies execute with 1 cycle throughput, 2 cycle latency
- Single-cycle MMX/FP context switch

Cyrix

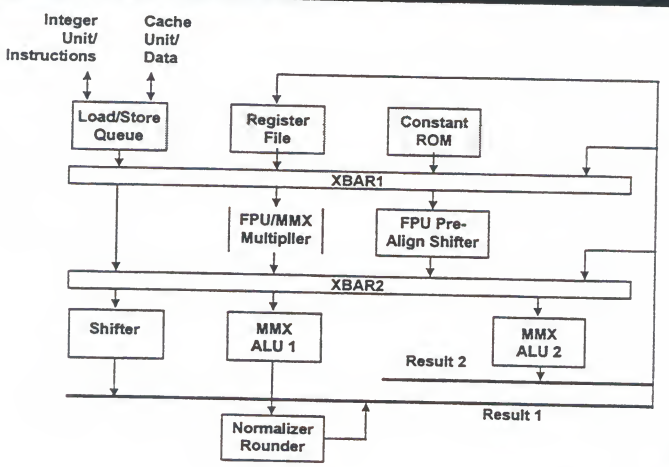
Cayenne Core: MMXFP

- Enhanced MMX execution unit
  - Additional data types
    - IEEE 754 single-precision floating point
  - Two single-precision floating point results per operation
  - Dual execute ⇨ 4 FLOPS per clock cycle
    - 1 FP add unit / 1 FP multiply unit

> 1 GFLOP peak performance

Cyrix

MMX and FPU Block Diagram



Cyrix

MMXFP Instruction Extensions

- Add, Sub, Multiply, Convert, and Compare operations which support FP data types
- Scatter/Gather operations for vectorized floating point
  - Gather and scatter triangle vertices for optimum parallelism
- Reciprocal and Reciprocal Square Root
- Motion Estimation Instruction

Cyrix

MMXFP: Software Support and Execution

- Work with Microsoft to support MMXFP in retained mode Direct3D driver
- Assist 3rd-party software development: i.e., game developers: immediate mode drivers

Throughput / Latency		
	MMX	Equiv x86FP
Load/Store/Convert	1/1	2/4
Add/Multiply	1/3	2/4
Reciprocal	3/5	48+/48+
Root Reciprocal	3/5	140+/140+

Cyrix

MMXFP: Geometry Transforms

$$[\,x'\ y'\ z'\ w\,] = [\,x\ y\ z\ 1\,] * T_{geom} * T_{view}$$

$$T_{geom} = \begin{vmatrix} a00 & a01 & a02 & 0 \\ a10 & a11 & a12 & 0 \\ a20 & a21 & a22 & 0 \\ tx & ty & tz & 1 \end{vmatrix} \qquad T_{orth} = \begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix} \qquad T_{pers} = \begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1/d \\ 0 & 0 & 0 & 0 \end{vmatrix}$$

- 4 x 4 matrix multiply reduces to 3x3 matrix multiply with a 3x1 vector add
- Translates 2 vertices at a time in 21 clocks
- 10.5 clocks/vertex vs. 36 clocks/vertex with standard x86 code

> 3x Performance Increase

Cyrix

MMXFP: Lighting Calculation

$$I_d = I_i * k_d * (L \circ N)$$

- I_i is the intensity at the light source
- k_d is a coefficient of diffuse lighting
- L is direction vector
- N is surface normal

- Processes 2 vertices in 23 clocks
- 11.5 clocks/vertex vs. 129 clocks with standard x86 code (70 clock square root)

>10 million meshed triangles / sec peak performance (Geometry + Lighting)

Cyrix

Summary

- 6x86MX™ to support 100 MHz socket 7 bus with state-of-the-art system features: AGP, SDRAM, 1394, Device Bay, ATA66
- Cayenne Core:
  - Dual-issue, pipelined FPU/MMX to enable highest performance 3D graphics, DVD, and 3D audio
  - MMXFP floating point extensions
  - PR300 to PR400
  - 65 sq mm in .25 um, 5 layer metal process
  - 2H98 production

Cyrix

An Enhanced C6-Family Microprocessor

Glenn Henry, *Centaur Technology*

presented by MICRODESIGN RESOURCES

PANEL

Design Challenges for Next-Generation x86 Microprocessors

Michael Slater, *moderator, MDR*
Robert Colwell, *Intel*
Greg Favor, *AMD*
Robert Maher, *Cyrix*
Glenn Henry, *Centaur Technology*

presented by MICRODESIGN RESOURCES

Motivations and Design Approach for a New 64-Bit Instruction Set Architecture

John Crawford, *Intel*
Jerry Huck, *Hewlett-Packard*

presented by MICRODESIGN RESOURCES

Next Generation Instruction Set Architecture

John Crawford, Intel Fellow
Director, Microprocessor Architecture
Intel Corporation

Jerry Huck
Manager and Lead Architect
Hewlett-Packard Company

Objectives

- **Unveil the technology behind the next generation ISA**
  - Today's focus on architecture, not implementation
- **Context**
  - History
  - Motivation
- **ISA Preview**
  - A few key features
  - Benefits

Intel and HP Technology Alliance

- **Intel**
  - Microprocessor / platform technology
  - 64-bit architecture definition
- **HP**
  - Enterprise systems technology expertise
  - Architecture research advancements
- **Jointly defined next generation 64-bit instruction set**
  - Instruction set specification
  - Compiler optimization
  - Performance simulation and projection

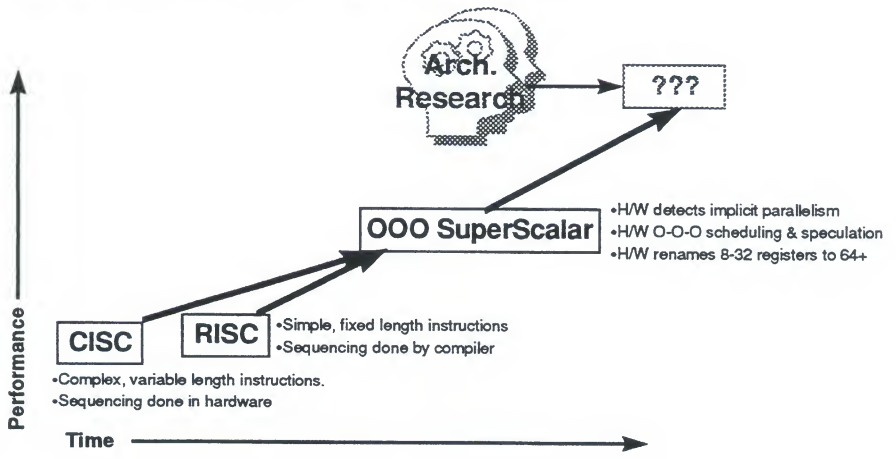
Intel — 3 — HEWLETT PACKARD

Instruction Set Architecture (ISA) Objectives

- **Enable industry leading system performance**
  - Breakthrough performance
  - Headroom
- **Enable compatibility with today's IA-32 software & PA-RISC software**
- **Allow scalability over a wide range of implementations**
- **Full 64-bit computing**

Intel — 4 — HEWLETT PACKARD

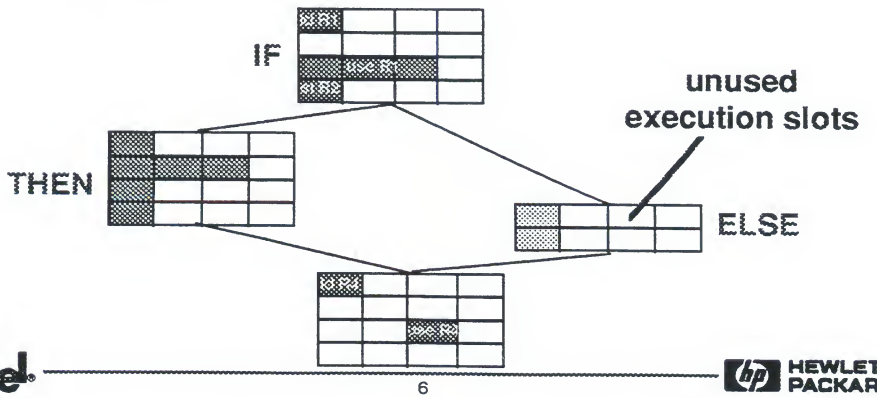
Current State of The Art



What's next, beyond traditional architectures?

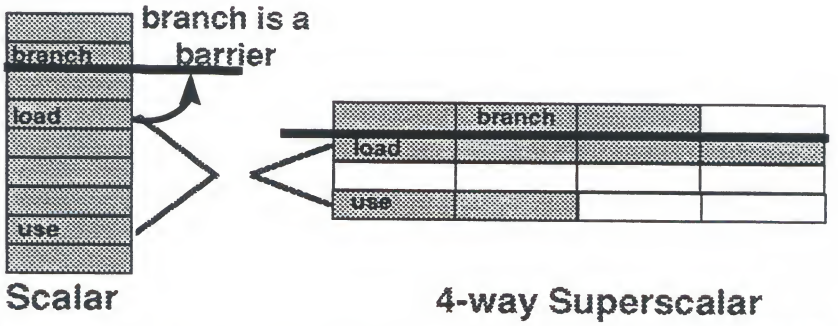
Current Performance Limiters:
Branches

- **Mispredicts limit performance**
- **Small blocks restrict code scheduling freedom**
  - Fragmentation
  - Poor utilization of wide machines



Current Performance Limiters:
Latency to Memory

- **Memory latency increasing relative to processor speed**
- **Load delay compounded by machine width**
  - Latency hiding requires more parallelism in a wide machine



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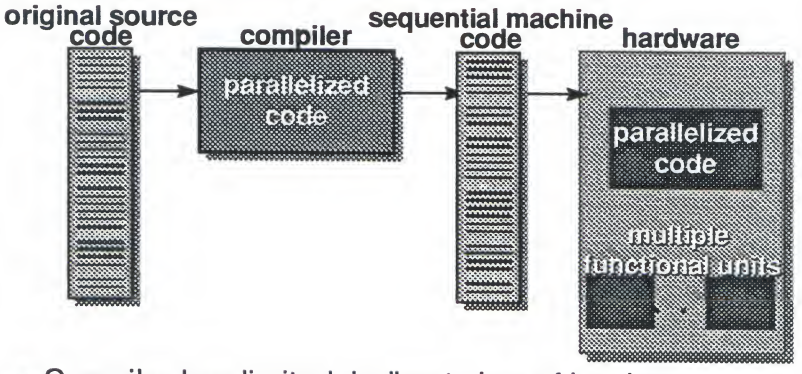
7

Current Performance Limiters:
Extracting Parallelism

- Sequential execution model



- Compiler has limited, indirect view of hardware

Implicit parallelism limits performance

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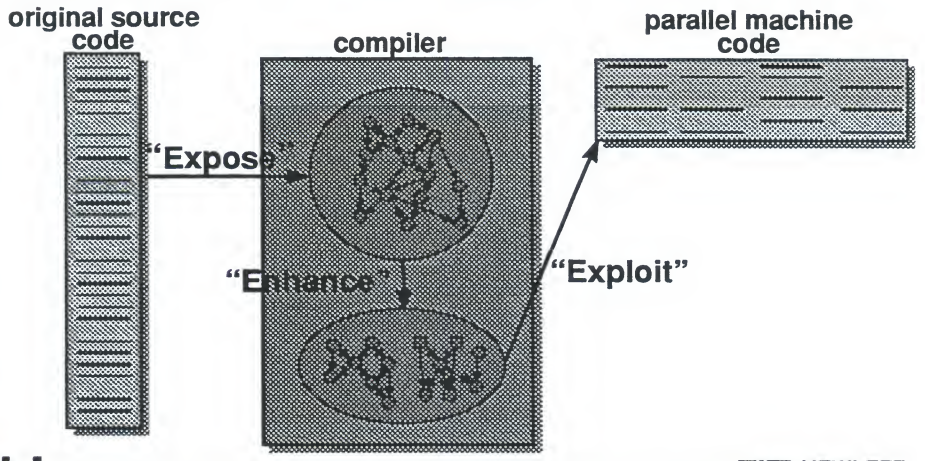
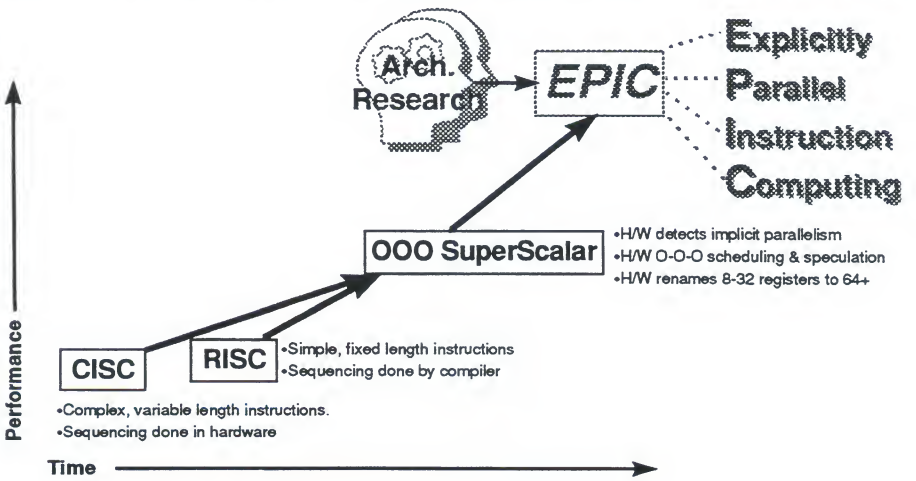
8

Better Strategy: Explicit Parallelism

Compiler exposes, enhances, and exploits parallelism in the source program and makes it explicit in the machine code.



Next Generation Architecture Technology



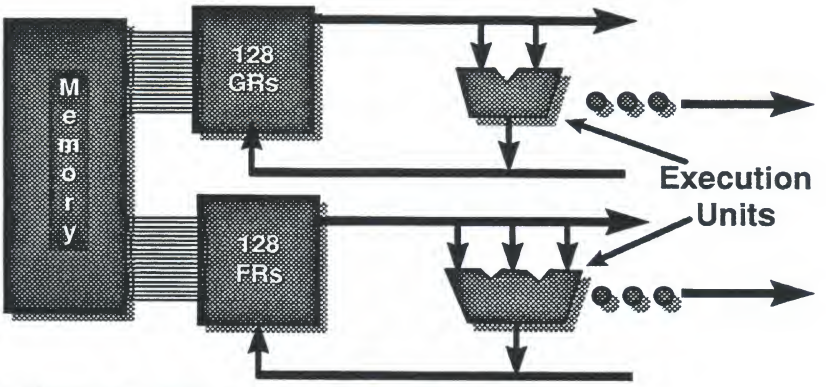
Next Generation Terminology

- **EPIC is the next generation technology**
  - e.g., RISC, CISC
- **IA-64 is the architecture that incorporates EPIC Technology**
  - e.g., IA-32, PA-RISC
- **Merced™ processor is the first IA-64 based implementation**
  - e.g., Pentium® II processor, PA-8500

Key 64-bit ISA Features within IA-64

- **Architecture Resources**
- **Instruction Format**
- **Predication**
- **Speculation**
- ***(Branch Architecture)***
- ***(Floating-Point Architecture)***
- ***(Multimedia Architecture)***
- ***(Memory Management & Protection)***
- ***(Compatibility)***

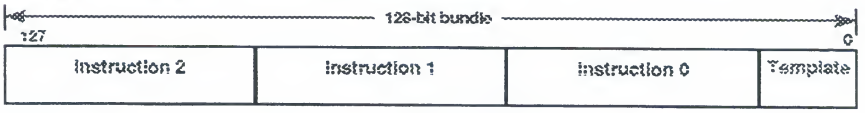
Architecture Resources Provide for Parallel Execution & Scalability



- Massively resourced - large register files
  - Traditional architectures are forced to rename registers
- Inherently scalable - replicated function units
- Explicitly parallel - transistors used more effectively

Instruction Format: Explicit Parallelism

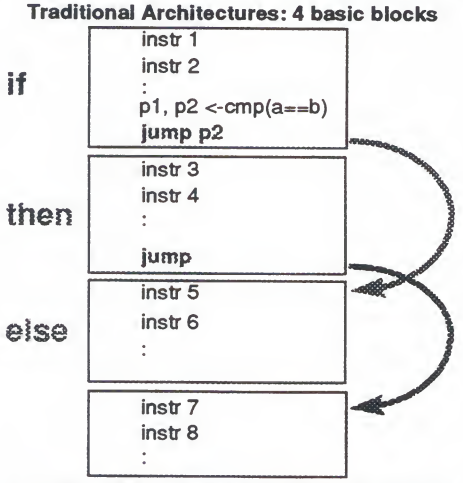
- **Breaking the sequential execution paradigm**
  - Explicit instruction dependency: template
  - Flexibly groups any number of independent instructions
- **Explicitly scheduled parallelism**
  - Enables compiler to create greater parallelism
  - Simplifies hardware by removing dynamic mechanisms
  - Fully interlocked- hardware provides compatibility



- **Modest code size expansion**

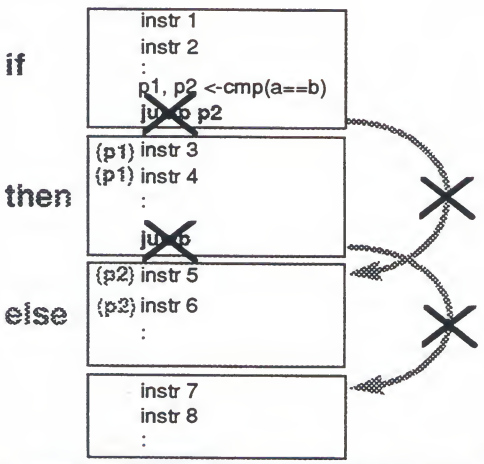
The new instruction format enables scalability w/ compatibility

Branches Limit Performance



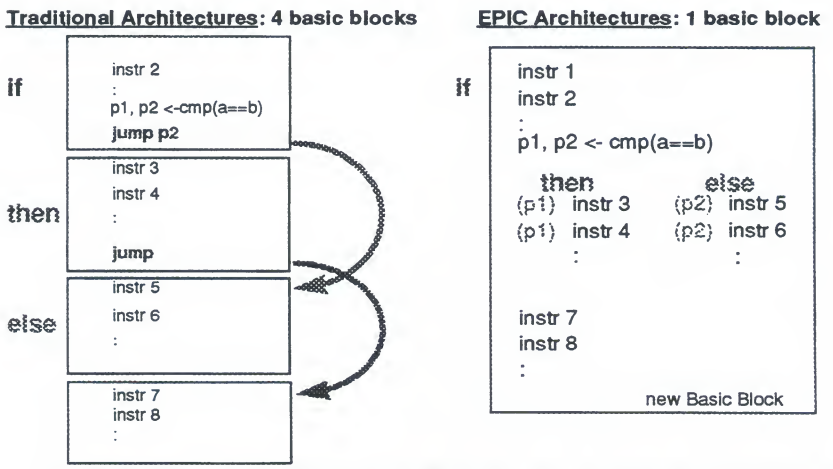
Control flow introduces branches

Predication



The predicate can remove branches

Predication Enhances Parallelism

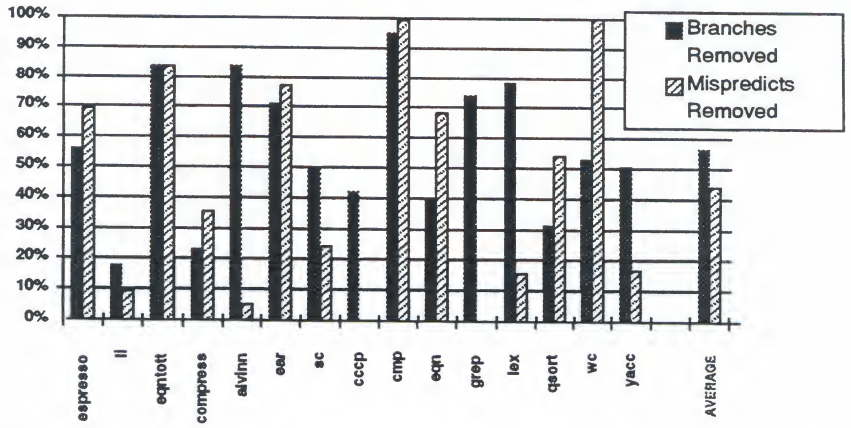


Predication enables more effective use of parallel hardware

Predication: Features and Benefits

- **Compiler given larger scheduling scope**
  - Nearly all instructions can be predicated
  - State updated if an instruction's predicate is true, otherwise acts as a NOP
  - Compiler assigns predicates, compare instructions set them
  - Architecture provides 64 1-bit predicate registers (PR)
- **Predicated execution removes branches**
  - Convert a control dependence to a data dependence
  - Reduce mispredict penalties
- **Parallel execution through larger basic blocks**
  - Effective use of parallel hardware

Predication Increases Performance

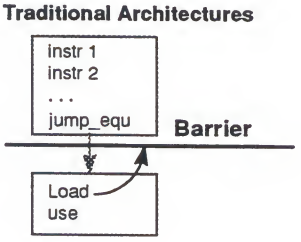


On average, over half of all branches are removed

Source: ISCA '95 S.Mahlke, et.al.

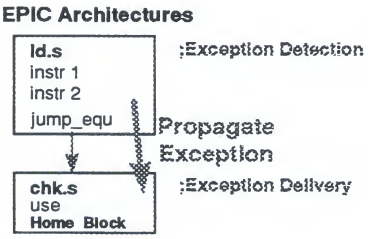
Memory Latency Causes Delays

- **Loads significantly affect performance**
  - Often first instruction in dependency chain of instructions
  - Can incur high latencies



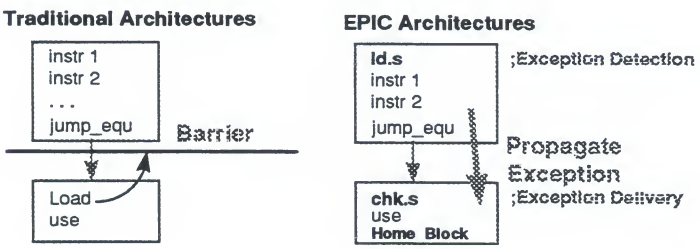
- **Loads can cause exceptions**

Speculation



- **Separate load behavior from exception behavior**
  - Speculative load instruction (ld.s) initiates a load operation and detects exceptions
  - Propagate an exception "token" (stored with destination register) from ld.s to chk.s
  - Speculative check instruction (chk.s) delivers any exceptions detected by ld.s

Speculation Minimizes the Effect of Memory Latency



- **Give scheduling freedom to the compiler**
  - Allows ld.s to be scheduled above branches
  - chk.s remains in home block, branches to fixup code if an exception is propagated

Example: 8 Queens Loop

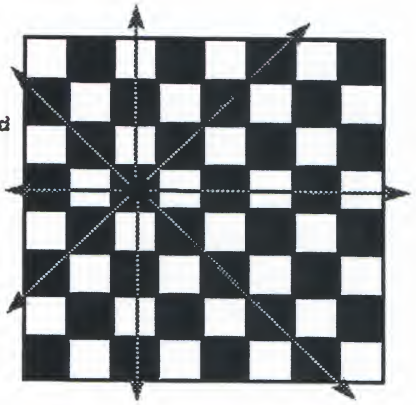
if ((b[j] == true) && (a[i+j] == true) && (c[i-j+7] == true))

Original Code

```
1   R1=&b[j]
    R3=&a[i+j]
    R5=&c[i-j+7]
2   ld R2=[R1]
4   P1,P2 <-cmp(R2==true)      True  Mispred
5   <P2> br exit               38%   43%

6   ld R4=[R3]
8   P3,P4 <-cmp(R4==true)
9   <P4> br exit               72%   33%

10  ld R6=[R5]
12  P5,P6 <-cmp(R5==true)
13  <P5> br then               47%   39%
    else
```



13 cycles
3 potential mispredicts

Example: 8 Queens Loop

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1   R1=&b[j]
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5   <P2> br exit

6   ld R4=[R3]
8   P3,P4 <-cmp(R4==true)
9   <P4> br exit

10  ld R6=[R5]
12  P5,P6 <-cmp(R5==true)
13  <P5> br then
    else
```

Speculation

```
1   R1=&b[j]
    R3=&a[i+j]
    R5=&c[i-j+7]
    ld R2=[R1]
2   ld.s R4=[R3]
    ld.s R6=[R5]
4   P1,P2 <-cmp(R2==true)
5   <P2> br exit

6   chk.s R4
    P3,P4 <-cmp(R4==true)
7   <P4> br exit

8   chk.s R6
    P5,P6 <-cmp(R5==true)
9   <P5> br then
    else
```

13 cycles
3 potential mispredicts

9 cycles
3 potential mispredicts

Example: 8 Queens Loop

if ((b[j] == true) && (a[i+j] == true) && (c[i-j+7] == true))

Speculation

```
1  R1=&b[j]
   R3=&a[i+j]
   R5=&c[i-j+7]
2  ld R2=[R1]
   ld.s R4=[R3]
   ld.s R6=[R5]
4  P1,P2 = cmp(R2==true)
5  <P2> br exit

6  chk.s R4
   P3,P4 = cmp(R4==true)
7  <P4> br exit

8  chk.s R6
   P5,P6 = cmp(R5==true)
9  <P5> br then
   else
```

Predication

```
1  R1=&b[j]
   R3=&a[i+j]
   R5=&c[i-j+7]
2  ld R2=[R1]
   ld.s R4=[R3]
   ld.s R6=[R5]
4  P1,P2 = cmp(R2==true)
   <P2> br exit
5  <p1> chk.s R4
   <p1> P3,P4 = cmp(R4==true)
   <P4> br exit
6  <p3> chk.s R6
   <p3> P5,P6 = cmp(R5==true)
7  <P5> br then
   else
```

True	Mispred
12%	16%

9 cycles
3 potential mispredicts

7 cycles
1 potential mispredict

Example: 8 Queens Loop

if ((b[j] == true) && (a[i+j] == true) && (c[i-j+7] == true))

Original Code

```
1  R1=&b[j]
   R3=&a[i+j]
10 ld R6=[R5]
12 P5,P6 = cmp(R5==true)
13 <P5> br then
   else
```

Predication

```
1  R1=&b[j]
   R3=&a[i+j]
6  <p3> chk.s R6
   <p3> P5,P6 = cmp(R5==true)
7  <P5> br then
   else
```

RESULT: Almost half the required cycles are reduced and 2/3 of the potential mispredicts are eliminated.

13 cycles
3 potential mispredicts

7 cycles
1 potential mispredict

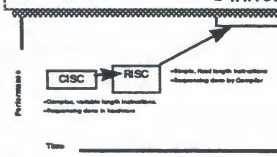
EPIC is the Next Generation Technology

Explicitly Parallel Instruction Computing

▲**Explicit parallelism**
- ILP is explicit in machine code
- Compiler schedules across a wide scope
- Binary compatibility across all family members

▲**Features that enhance ILP**
- Predication
- Speculation
- Others...

▲**Resources for parallel execution**
- Many registers
- Many functional units
- Inherently scalable



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IA-64: EPIC Technology Applied

▲**Enables industry leading performance and capability**
- Explicitly parallel: Beyond the limitations of current architectures
- Inherently scalable, massively resourced: Provides headroom for future market requirements
- Fully compatible: For existing applications and the future

▲**Addresses server and workstation market requirements**
- Enterprise transaction processing
- Decision support
- Graphical imaging
- Volume rendering
- Many others

The Next Generation in Computer Architecture

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PANEL

Motivations and Design Approach for a New 64-Bit Instruction Set Architecture

John Crawford, *Intel*
Jerry Huck, *Hewlett-Packard*

presented by MICRODESIGN RESOURCES

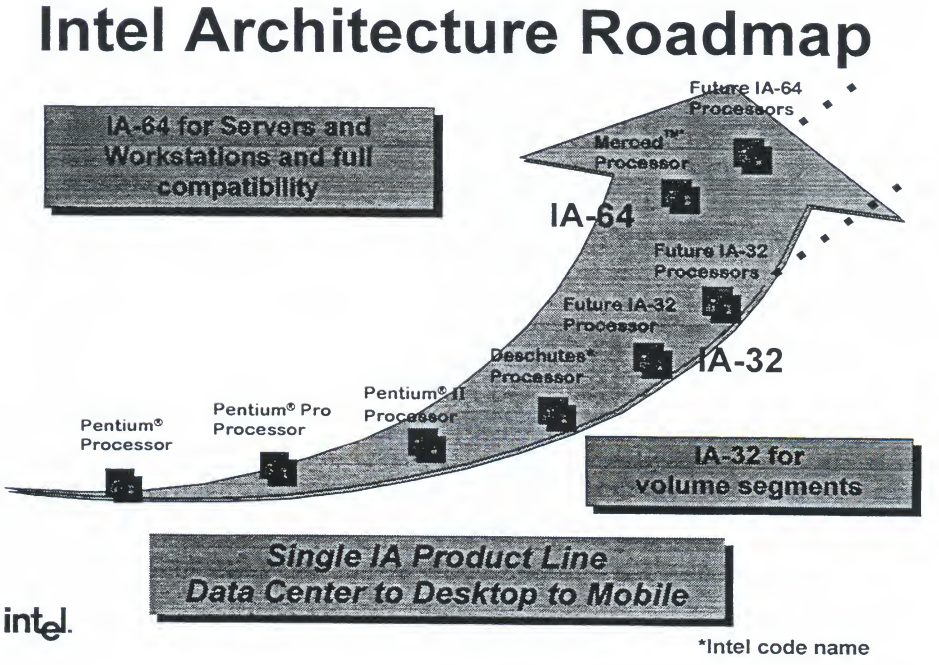
Intel Architecture Roadmap

Fred Pollack, *Intel*

sponsored by MICRODESIGN RESOURCES

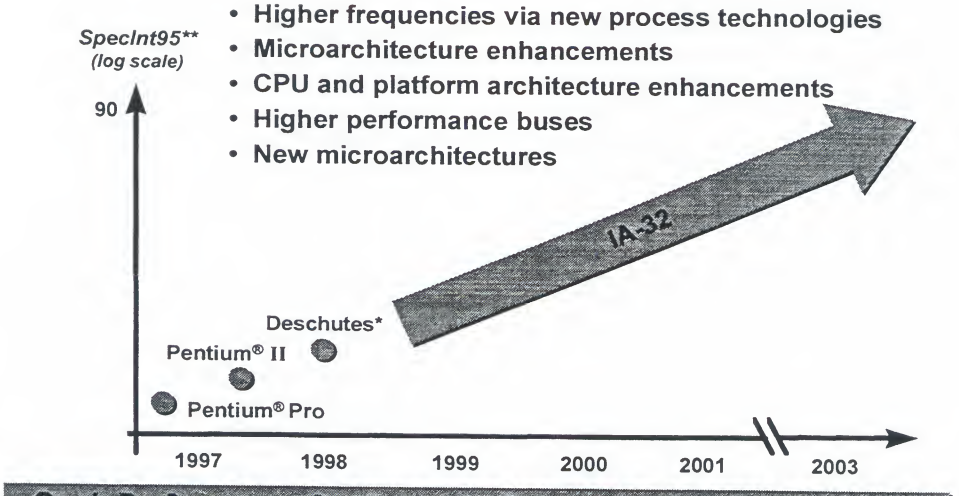
Intel Architecture Roadmap

Fred Pollack
Intel Fellow
and
Director of Processor Planning for
Intel's Microprocessor Products Group



IA-32 Roadmap

- Higher frequencies via new process technologies
- Microarchitecture enhancements
- CPU and platform architecture enhancements
- Higher performance buses
- New microarchitectures



Goal: Performance Continues to Grow at Intel's Historical Rates

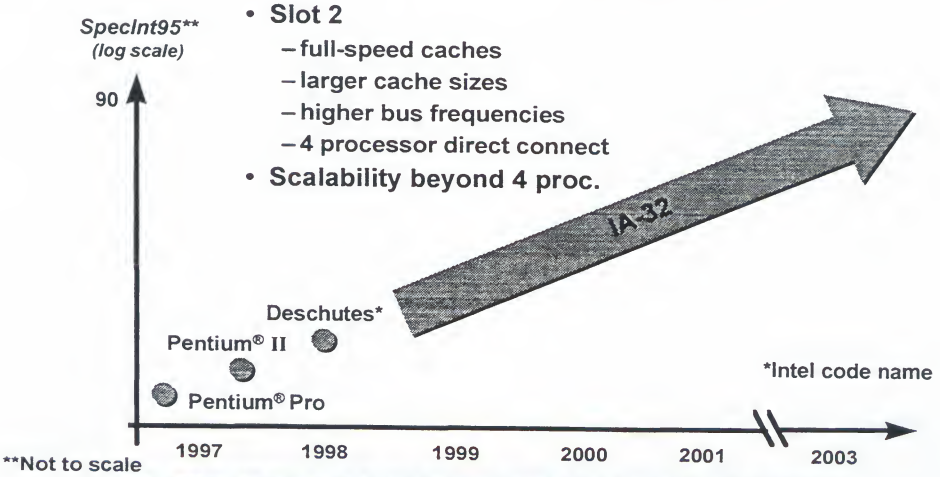
intel

**Not to scale

*Intel code name

IA-32 Server & Workstation

- Slot 2
  - full-speed caches
  - larger cache sizes
  - higher bus frequencies
  - 4 processor direct connect
- Scalability beyond 4 proc.



*Intel code name

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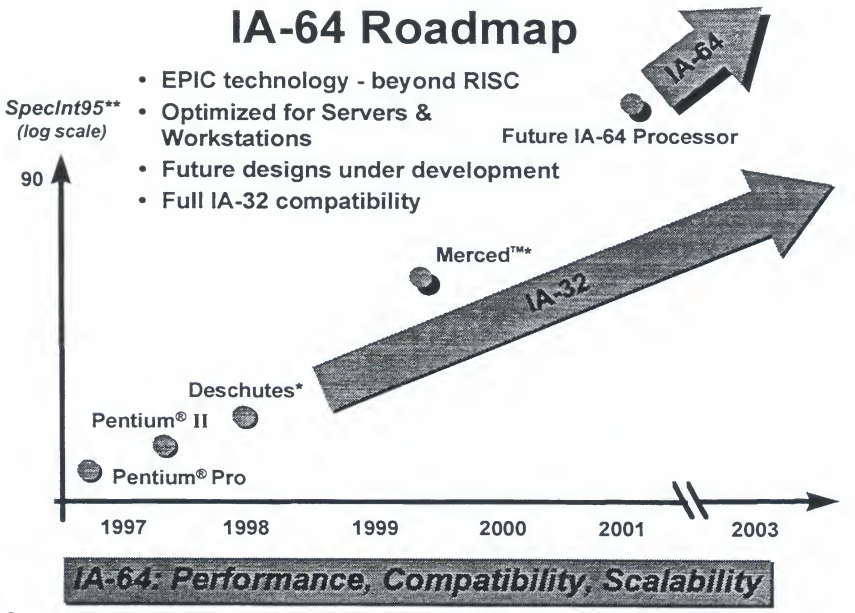
intel

Goal: Continue to Deliver Best Price/Performance for Servers & Workstations

IA-64 Roadmap



intel

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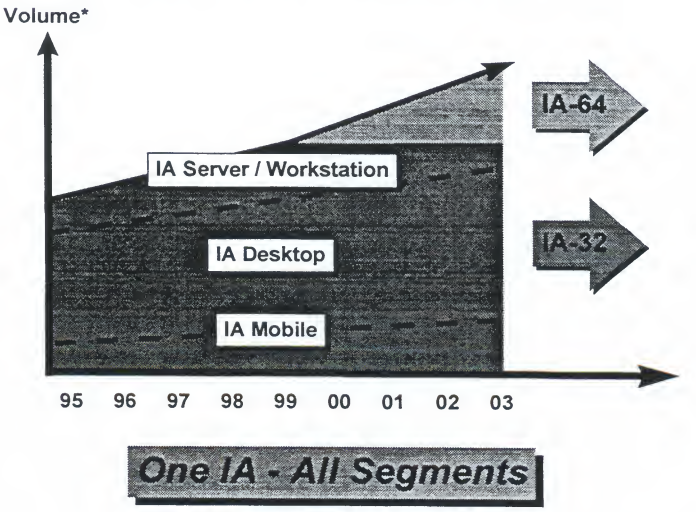
*Intel code name

Intel Architecture



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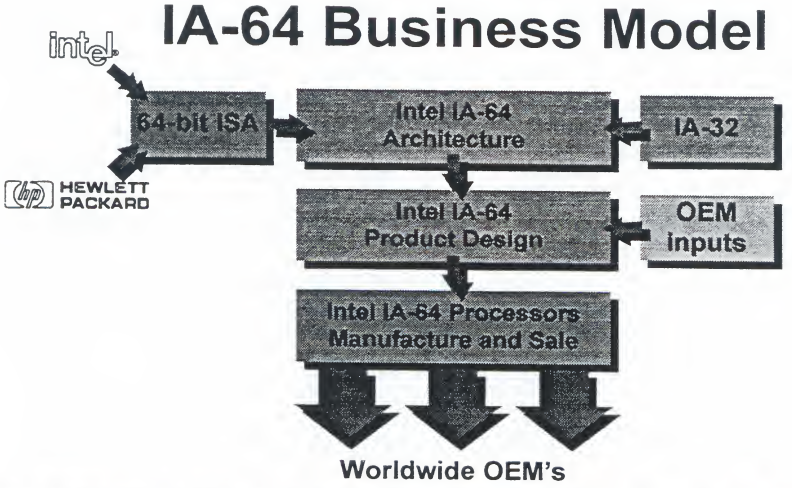
*Not to scale, for illustrative purposes only

IA-64 Business Model



IA-64 processors will be available to OEM's consistent with Intel's standard business practices

intel

Merced™ Processor - Program Update

- Merced™ Processor
  - Code name for Intel's first IA-64 processor
  - Industry leading performance and features for Servers and Workstations
  - Full IA-32 binary compatibility in hardware
  - Intel's 0.18 micron process technology
  - Multiple product configurations to address specific segment needs
- Complete solution stack at launch
  - Processor and chipset design teams on track for '99 production
  - OEM system design teams are making significant progress
  - Operating systems and key applications on track for launch

Merced™ Processor: Full speed ahead for 1999 production

intel

IA-64 Industry Commitment

Strong Industry Momentum

intel

Summary

- IA-32 continues to offer high performance solutions for Servers, Workstations, Desktops and Mobile
- IA-64 extends IA in high performance Servers and Workstations with full compatibility
- Continuing major investments in both IA-32 and IA-64

Advancing the future of computing

intel

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TENTH ANNIVERSARY

PANEL

Intel Architecture Strategies for High-Performance Computing

presented by MICRODESIGN RESOURCES

Architecture at HP: Two Decades of Innovation

Joel Birnbaum, *Hewlett-Packard*

sponsored by MICRODESIGN RESOURCES

Architecture at HP: Two Decades of Innovation

Joel S. Birnbaum

Microprocessor Forum
San Jose, CA
October 14, 1997

JBTALKS/MPF1097/MPF1097.PPT

Computer Architecture at HP

- A summary of motivations, innovations and implementations in the period 1981 to the present
- Some observations about emerging systems requirements for the next decade and ongoing research to address them

JBTALKS/MPF1097/MPF1097.PPT

A Capsule History

The 80s:

- RISC consolidation and evolution
- Spectrum, HP Precision Architecture, and PA-RISC
- Migration from HP 3000, 1000, M68000 architectures

The Early 90s:

- Beyond RISC: The quest for concurrency
- Superscalar, VLIW, Wide Word
- Compatibility with PA-RISC

1994 - Present:

- The Intel alliance
- Next generation technology and IA-64

WHAT'S NEXT?...

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Precision Architecture Principles

- Compiler does what it does best
- Hardware does what it does best
- As simple as possible, but not simpler
- Measure / justify everything
  - Optimize for application throughput
  - Most work in least time
- Architecture scales across family of implementations
- Seamless migration essential

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Technology Enablers of RISC Architecture

- Progress in VLSI: Fast registers, cache
- Globally optimizing compilers
- Performance measurement and analysis tools

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Challenges of RISC Architecture

- Compiler accuracy and reliability
- Migration of legacy code

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Major PA-RISC Innovations

- Compound instructions based on usage statistics
- Instruction nullification
- Legacy software migration
  - Binary code translation
  - Millicode
  - Migration centers
- 64-bit addresses
  - 32-bit segments
- Graphics and multimedia extensions

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Why a New Architecture?

- Insatiable demand for more performance
- Processor/memory speed gap implications
  - Higher bandwidth
  - More registers
  - Overlapped memory latencies
- Need for greater number of instructions per cycle
- Diminishing gains from growing microprocessor design complexity

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Industry Solutions

- Superscalar RISC
  - Improved ILP, but:
    - Significant hardware complexity
    - Not transparent to compiler
    - Asymptotic IPC of 1.5 - 3
- VLIW, Vector Architectures
  - Even higher ILP
    - Explicit parallelism
    - Parallelizing compilers
  - But limited applicability, scalability, and compatibility
- Drives the need for a new architecture

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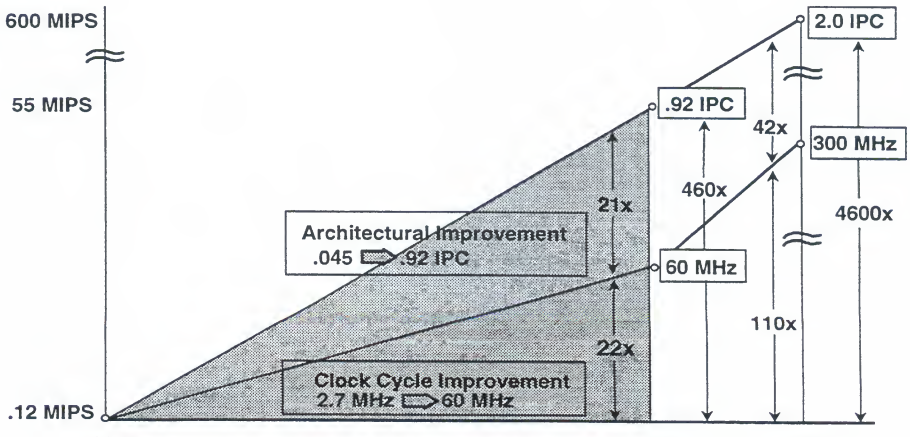
Microprocessor Performance Growth



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Source: IEEE Spectrum (1989) (1976-1993)

Major Conclusion: High ILP Needs a New Architectural Approach

- High ILP requires explicitly scheduled code
  - Scheduling by compiler
- Architecture must expose parallelism
- Scalability across implementations and applications required

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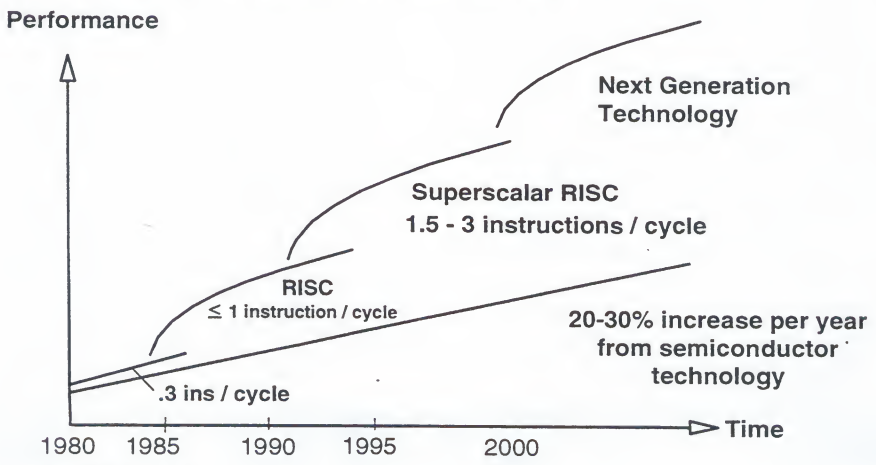
IPC Evolution from Architecture and Microarchitecure



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Need for a New Industry-Standard Architecture

- HP alone would not succeed with a new proprietary architecture: economics, acceptance by ISVs
- Technology alliance melds architecture/ design / fabrication excellence of Intel with architecture and systems excellence of HP
- Opportunity for scalable common hardware platforms across operating systems

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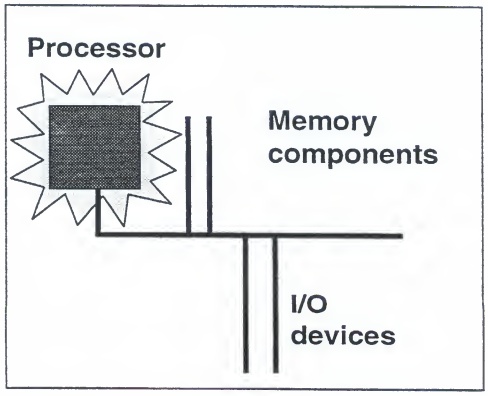
The Rest of the System?



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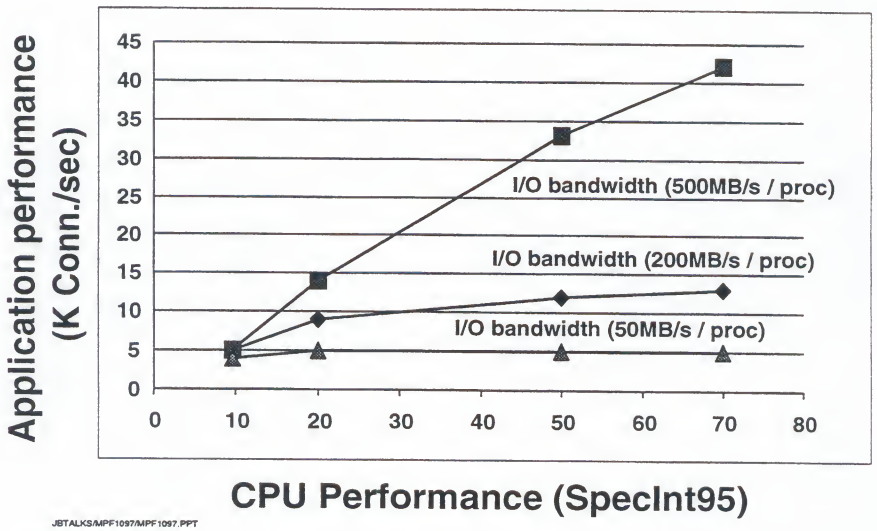
The Rest of the System



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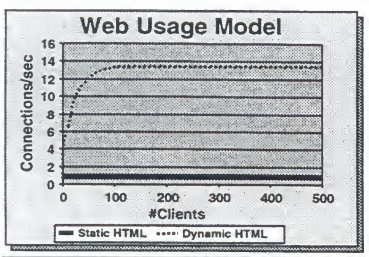
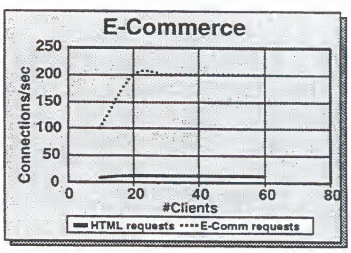
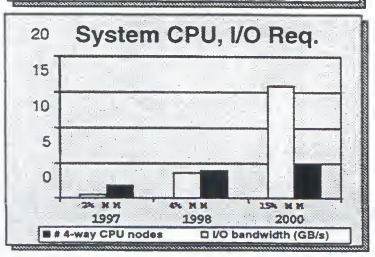
Changing Workloads



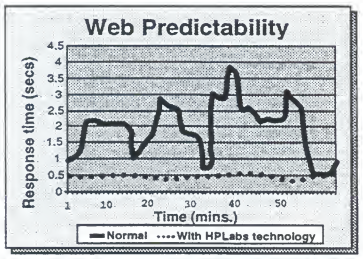


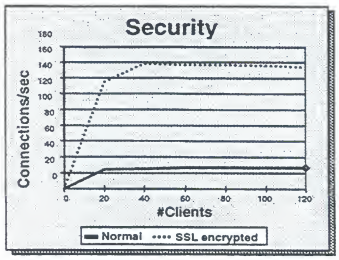


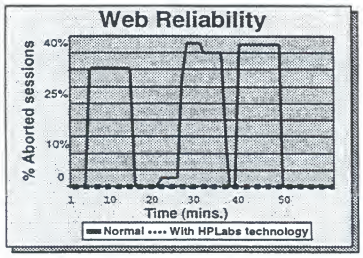
- *Increasing system loads*
- *Increasing system bandwidth requirements*

JBTALKS/MPF1097/MPF1097.PPT

New Cost-Value Measures







- *Need mechanisms for predictability, security, reliability*

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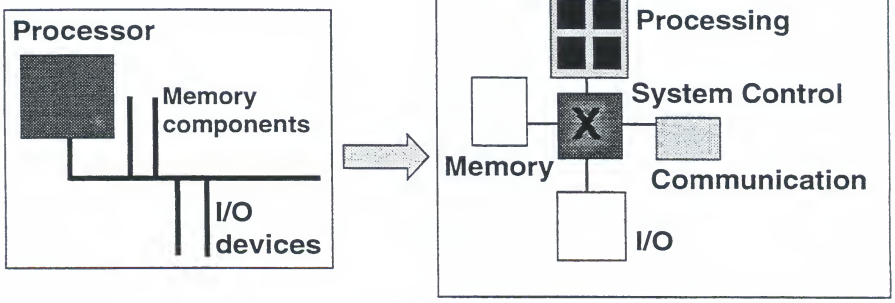
New Control Points

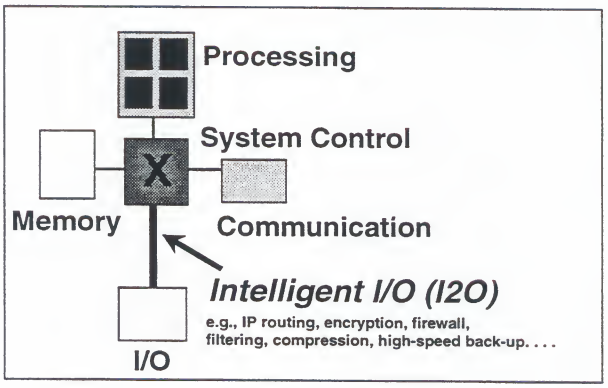


Processor-centric ⇒ Semi-autonomous Subsystems

JBTALKS/MPF1097/MPF1097.PPT

New Control Points

... in an open industry standard framework that permits system value adds



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The New Challenges

Computing Components

- Semi-autonomous subsystems
- Integrated communication, memory, and computation

Computing Systems

- Distributed, heterogeneous systems of systems

Computing Services

(Information and Computation "Utilities")

JBTALKS/MPF1097/MPF1097.PPT

The New Challenges

Computing Components

- Custom (embedded) processors
- New control points

Computing Systems

- Information appliances
- Utility servers

Computing Services

(Information and Computation "Utilities")

JBTALKS/MPF1097/MPF1097.PPT

The New Challenges

Computing Components

- Custom (embedded) processors
- New control points

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- Integrated communication, memory, and computation

Computing Systems

- Information appliances
- Utility servers

- Distributed, heterogeneous systems of systems

Computing Services

(Information and Computation "Utilities")

HP Labs is focused on the new challenges of tomorrow

JBTALKS/MPF1097/MPF1097.PPT

The Evolving RISC Landscape

Linley Gwennap,
Microprocessor Report

presented by MICRODESIGN RESOURCES

The Evolving RISC Landscape

Linley Gwennap
Senior Analyst
MDR

Changes in the Past Year

- HP, Digital contend for integer lead
  - Despite lagging IC technology
- First 0.25-micron chips appeared
  - IBM, Motorola, TI lead the way
  - Need new core for best performance
- Intel gained momentum, design wins at key RISC strongholds
  - Apple, Tandem, Silicon Graphics

What DIDN'T Happen

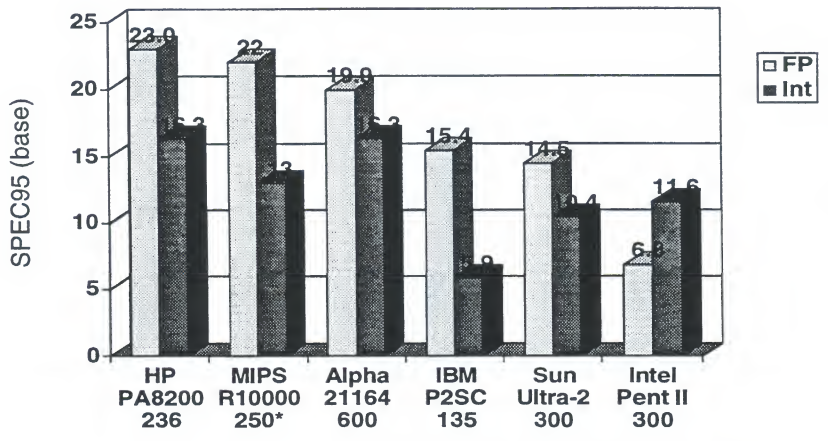
- No new high-end cores shipped
  - PowerPC 750 shipped, but not high end
  - PA-8200 offers only minor changes
- 21264 didn't meet schedule
  - Tape-out delay puts shipments to 2Q98
- Exponential didn't survive
  - Bipolar hopes extinguished

RISC System Consolodation

- RISC market continues to grow
  - $51.7 billion in system sales in 1996*
  - 24% growth over previous year*
- Few vendors use RISC other than processor developers
  - No NT on MIPS, PowerPC
  - Apple closes Mac clone market
  - Compaq moves Tandem from MIPS

*Source: Andrew Allison

RISC Drives FP Performance



(Source: SPEC except *vendor estimates)

RISC Drives CPU Design

- Dual-issue floating-point
  - Two independent 64-bit FP ops/cycle
  - Sometimes dual FP MAC (4 FP ops/cyc)
- More on-chip cache
- More memory bandwidth
  - GBytes/s versus Intel's 528 Mbytes/s
- Better MP scalability

What to Watch For in 1998

- Leading RISC processors deliver 30+ SPECint95, 50+ SPECfp95 (base)
  - Twice Intel's best performance in 1998
- HP continues to vie with Digital for integer performance lead
- Others will lag in performance
- RISC processor designs focus on transaction and scientific servers

Sun's Next-Generation High-End SPARC Microprocessor

Gary Lauterbach,
Sun Microsystems

presented by MICRODESIGN RESOURCES

UltraSPARC - III

A Scalable High Clock Rate SPARC Processor

Gary Lauterbach
Sun Microsystems, Inc.

US-III Goals and Motivations

Motivations:

- Memory sub-system is key to scalable performance
- Wire delays dominate cycle time

Goals:

- Industry-leading memory and system bandwidths
- Performance scaling on existing binaries
- Industry-leading system scalability: 1000+ processor systems
- Rapid performance scaling with future process technology
- Full Sparc V9 and Solaris compliant

Overview

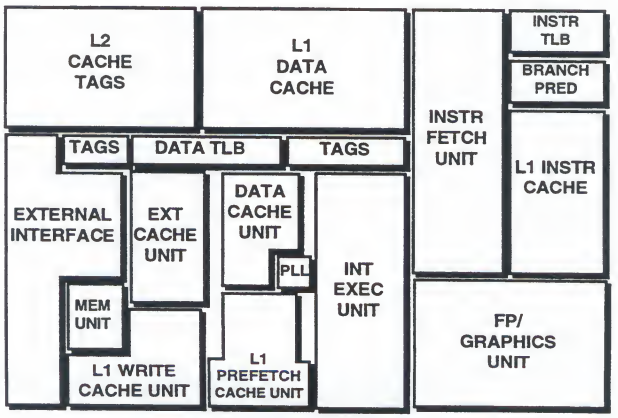
Physical Characteristics

Process	.25µ CMOS 6 layer metal
Clock	600+ Mhz
Die Size	330 mm2
Power	70w@1.8volts
Transistor Count	RAM 12 million Logic 4 million
Package	1200 pin LGA

Pipeline Characteristics

Issue	4 Integer 2 Floating Point 2 Graphics
L1 Caches	64KB - 4 way Data 32KB - 4 way Instruction 2KB - 4 way Prefetch 2KB - 4 way Write
L2 Cache	1, 4, 8MB - 1 way On-chip Tags Off-chip Data

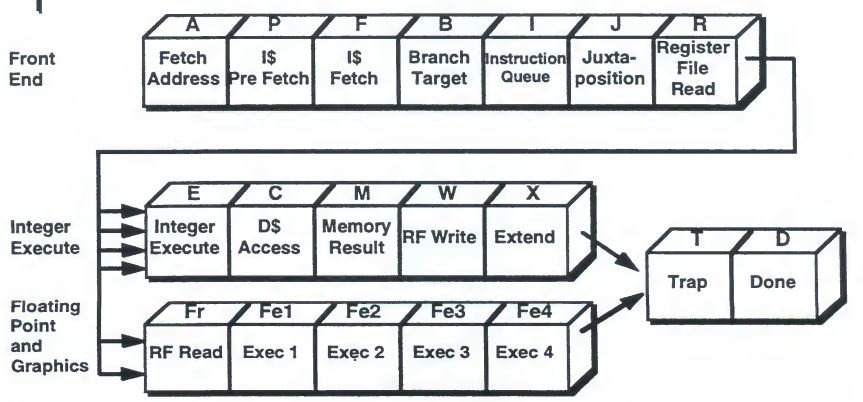
US-III Floorplan



Pipeline Features

- Est. 35+ SPECint95, 60+ SPECfp95 @ 600MHz (Base)
- 14 stage non-stalling pipeline
- Low latency, large, multi-set L1 data cache
- Extensive hardware/software prefetch support
- Fully integrated system and memory interfaces
- Code schedule compatible with UltraSPARC-I, II
- System software compatible with UltraSPARC-I, II

Pipeline Diagram



Instruction Fetch

- 32KB 4-way associative instruction cache
  - Fetch any 4 instructions in a 32 byte line
  - Virtual address micro-tags
  - 32 byte line size, 2 ns access time
- 16K entry history-based branch predictor
  - modified gshare with 12 global history bits and 14 branch PC bits, 2 bits per entry
- Branch mispredict cost
  - 7 cycles max
  - 3 cycles average mispredict taken
- 8 entry jump target/return address stack
- 20 entry instruction queue
- 4 entry miss queue
  - Saves fall-through path from mispredicted taken branches

Instruction Fetch

- 32KB 4-way Associative Instruction Cache
- 16K Entry History-based Branch Predictor
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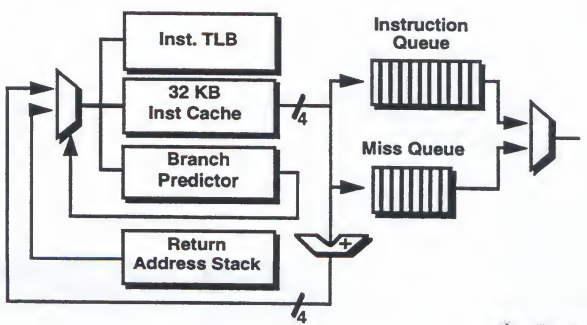
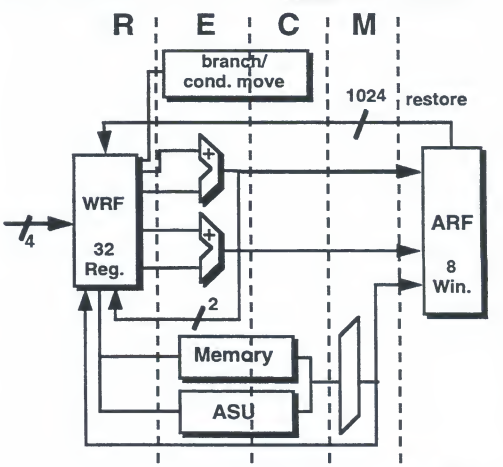


Integer Execute

- 4 integer issue from:
  - 2 Arithmetic/Logical/Shift
  - 2 Loads
  - 1 Store
  - 1 Branch
- Arithmetic/Special Unit (ASU)
  - 6-9 cycle integer multiply
- Pipelined predicated execution
  - 1 conditional move/cycle
- 7R3W port Register File
  - 1024 bit window change/restore
  - WRF - single window Working Register File
  - ARF - 8 window Architecural Register File



Floating Point/Graphics Execute

- 2 instruction issue from:
  - FP/graphics add
  - FP/graphics mul/div/sqrt
- Fully pipelined FP/graphics add/mul
- Concurrent FP div/sqrt unit
- 5 Read, 4 Write port register file

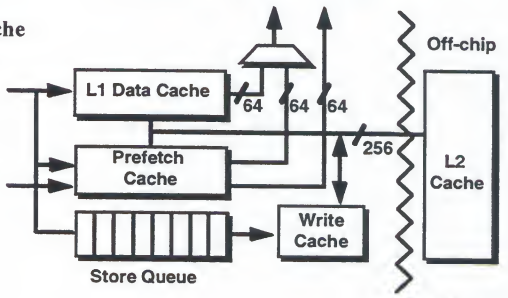
Instruction Latency

Instruction	Latency	
Graphics Add	4 cycles	
Graphic Multiply	4 cycles	
	Single	Double
FP Add	4 cycles	4 cycles
FP Multiply	4 cycle	4 cycle
FP Divide	17 cycle	20 cycle
FP Square Root	24 cycle	24 cycle

Memory Subsystem

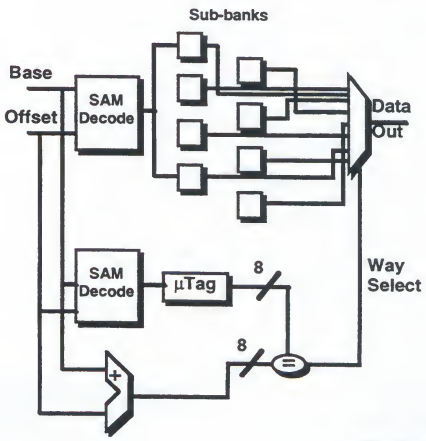
- 64KB 4-way associative L1 data cache
  - 32 byte line size
  - Virtual indexed, physically tagged
  - Write-through
- 2KB 4-way associative L1 prefetch cache
- 2KB 4-way associative L1 write cache
- 1-8 MB direct-mapped L2 cache
  - ECC protected
  - 256 bit datapath, 12 cycle latency
  - 3 or 4 cycle pipelined access
  - Level 1 caches are non-inclusive
  - 90KB on-chip L2 Cache tags
- 8 entry RAW forwarding store queue
- On-chip DRAM controller

Cache	Latency	Bandwidth
L1 Data	2 cycles	9.6 GB/s
L1 Prefetch	3 cycles	18.4 GB/s
L1 Write	1 cycles	13.6 GB/s
L2 External	12 cycles	6.4 GB/s



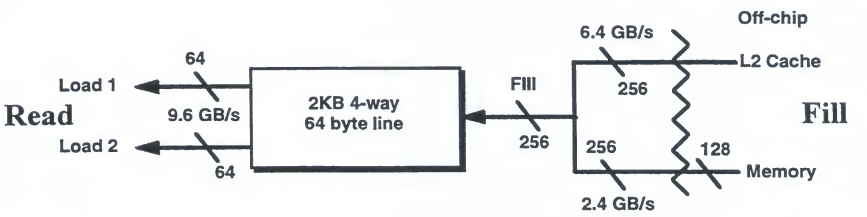
Data Cache

- Sum Addressed Memory(SAM)
  - Eliminates address adder from load path
  - 2 gate delays in address decode
  - No carry propagation
  - 1 load bubble
- Micro-Tags
  - 4-way associativity without access time penalty
  - 8-bit virtual address tag used to select way
  - Full physical address used to detect cache miss



Prefetch Cache

- Concurrent fill and dual reads
- 8 outstanding software prefetches
- Autonomous hardware stride prefetch
- Fully coherent cache



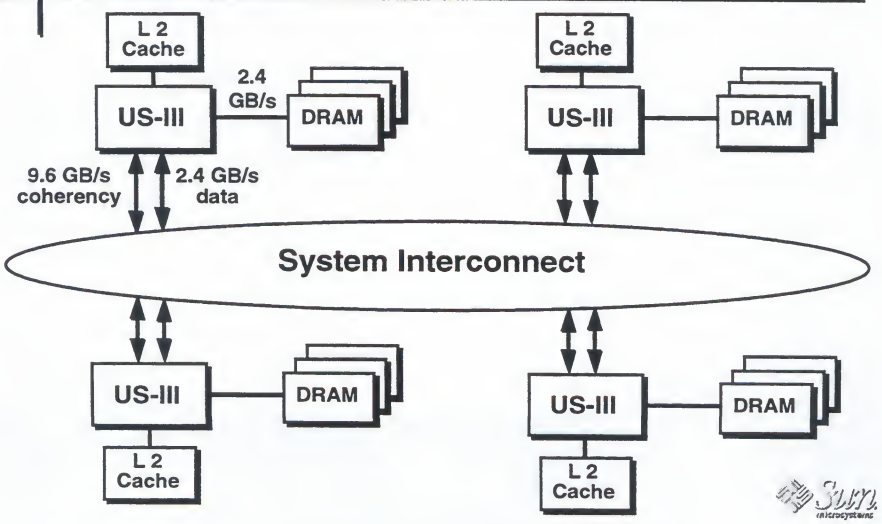
Multi-processor Scalability

- DRAM controller per processor
  - Fully programmable timing, interleave, etc.
  - 4 banks of DRAM, 4 GB max, 170 ns cycle miss latency
  - System memory bandwidth scales with number of processors
- Low memory latency
  - Minimum latency up to 4 processors
  - Small latency increase to 32 processors
  - Cache to cache transfers lower latency than memory
- Large Multi-processor scaling to 1000+ processors
  - Minimum overhead, several hundred gates

External Interface

- Coherency BW scales with processor technology
  - On-chip snoop tags (50%BW of L2 on-chip tags)
- 9.6 GB/s coherency bandwidth
  - High frequency, single cycle request
  - Distributed request arbitration
- 2.4 GB/s off-chip bandwidth
- Up to 15 outstanding transactions
  - Tagged transactions, out-of-order completion
  - Full V9 total-store-order compliance
- Independent boot/diagnostic bus

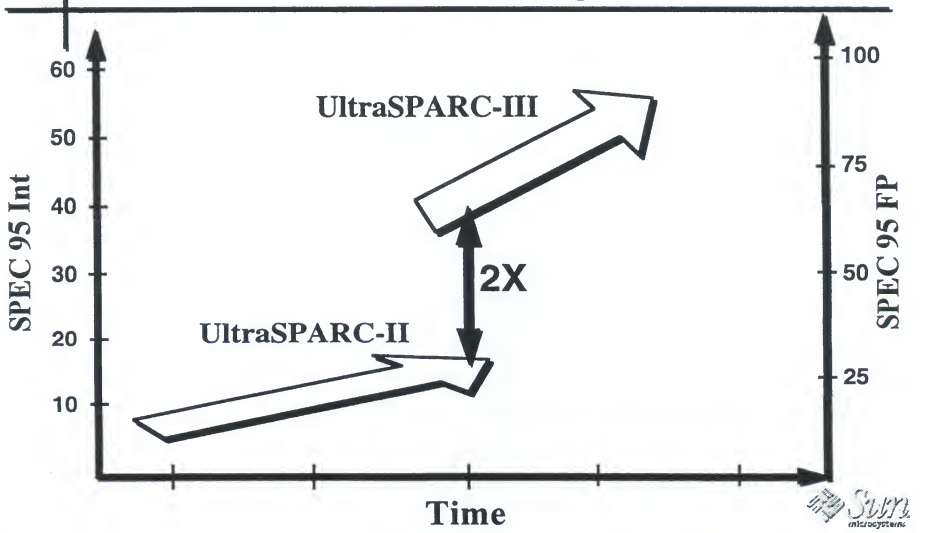
Example N Way System



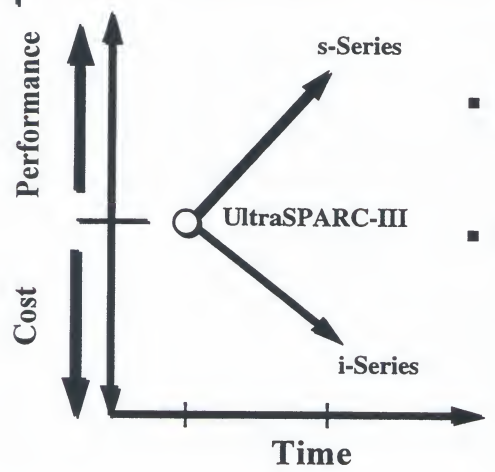
Application Enhancements

- Media enhancements:
  - VIS extension - byte mask/shuffle, pipelined alignment
- Scientific enhancements:
  - Rounding mode support for interval arithmetic
- JAVA acceleration:
  - Jump target preparation
  - Coherent instruction cache
- Networking acceleration:
  - "No snoop" page attribute
  - Multiple outstanding Block stores - 2.4GB/s block copy bandwidth

UltraSPARC Roadmap



Futures



- Derivative Products
  - Frequency & performance increase
  - Cost engineered
- Architecture Extensions
  - Java
  - Media

Summary

- Spectacular performance with full compatibility
  - Full SPARC V9, Solaris and code schedule compatibility with US-I, II
- Scalable performance on existing binaries
- Industry leading scalability: 1000+ processors
- Industry leading system and memory bandwidths
- Performance scaling with future process technology
- Numerous application-specific performance enhancements

A Next-Generation 64-Bit PowerPC Microprocessor

Mark Papermaster, *IBM*

presented by MICRODESIGN RESOURCES

POWER3

Next Generation 64-bit PowerPC Processor Design

Mark Papermaster
High-performance Processor Design
IBM Microelectronics
Austin, Texas

Microprocessor Forum
October 14, 1997

IBM

Agenda

IBM

- POWER3 Project Goals
- Microprocessor Roadmap
- Key Product Specs
- Processor Overview
- System Implementation
- Verification
- Performance
- Status & Future Directions

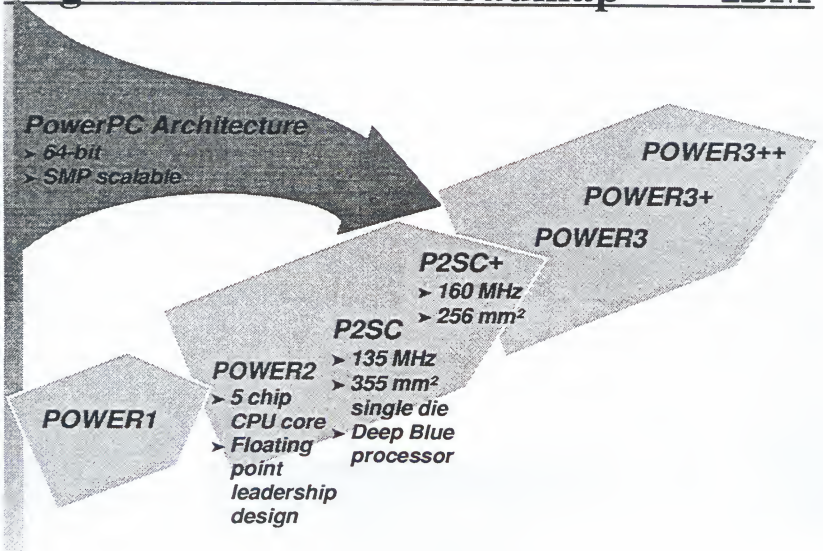
Goals

IBM

- Product
  - Outstanding system-level performance for workstations, servers, super computers
  - Mission critical applications, i.e. mechanical CAD, data mining, seismic analysis, OLTP
  - Build on POWER2 strengths with PowerPC architecture, SMP scalability, 64-bit
- Processor
  - *Bandwidth, memory system and dispatch capability to feed a highly superscalar execution core*
  - *Four floating-point operations per cycle*
- Technology
  - Introduce in established technology; rapidly advance to CMOS 7S technology

High-end Processor Roadmap

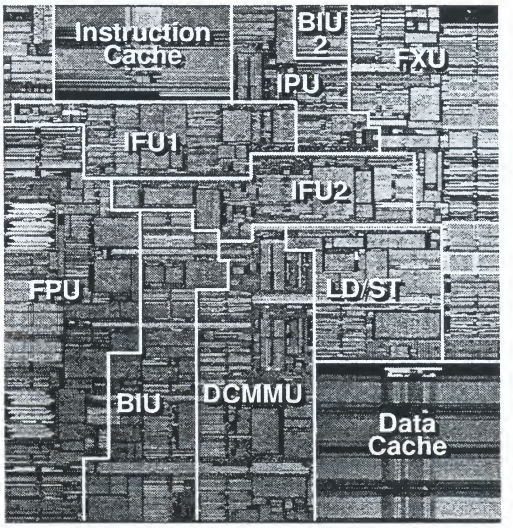
IBM



Key Product Specifications

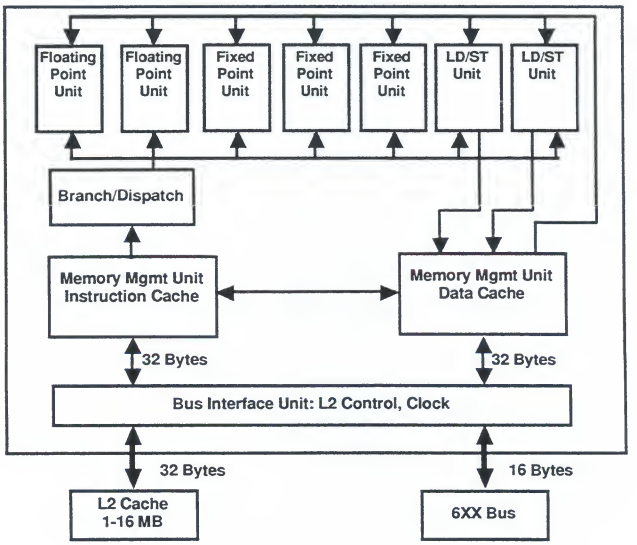
IBM

- Size & power
  - 15 million transistors
  - Die: 270 mm²
  - 46W
- Technology
  - CMOS 6S2
  - 0.25 µm hybrid lithography
  - Five levels of metal
  - 2.5 volts
- Package
  - 1088 pin ceramic package
  - 748 signal I/O
- Clock distribution
  - <100psec skew at latches



Superscalar Processor

IBM



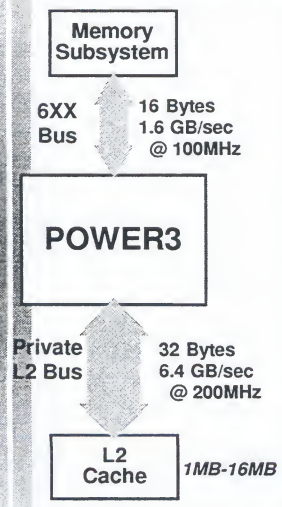
Execution Core

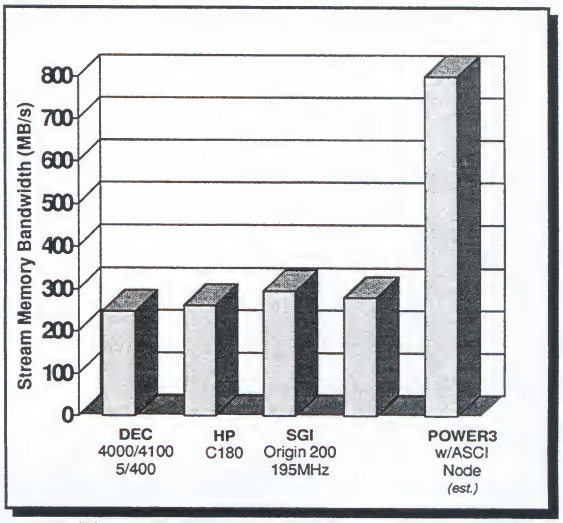
IBM

- Three fixed point units
  - Two units implement single cycle operations
  - One unit for complex, multi-cycle instructions
- Two floating point units
  - Double precision data path
  - Three cycle latency, one cycle throughput
  - Each unit contains divide and square root sub-units
  - 24 real and 32 virtual rename buffers
- Two load / store units
  - Each unit calculates one load or store / cycle
  - Loads processed speculatively
  - 16 entry store queue
- Branch unit
  - 2048 entry branch history table
  - 128 x 2 entry branch target cache
  - Four pending predicted branches

System Level Bandwidth

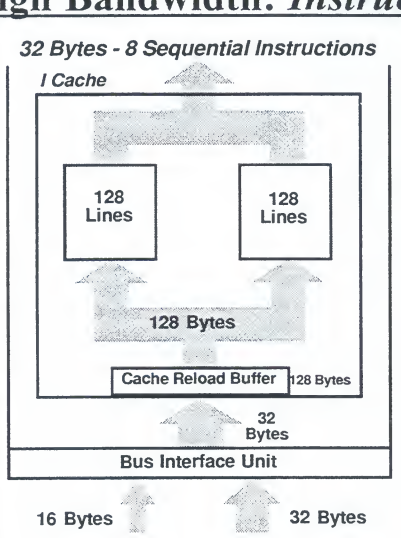
IBM





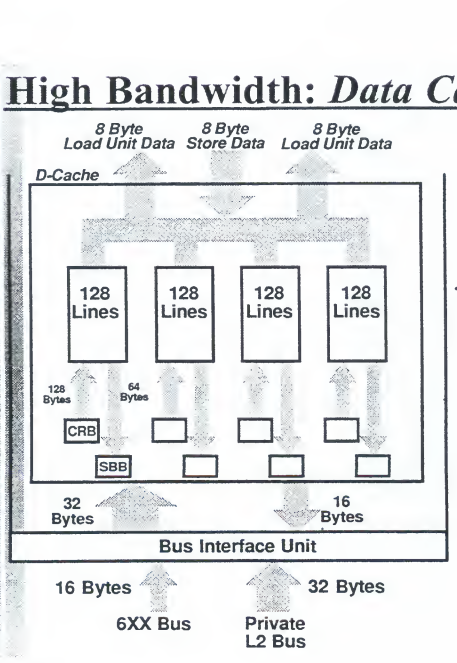
Performance data as of 9/97, as reported in corporate websites and other public sources; except IBM data, which is estimated.

High Bandwidth: *Instruction Cache*



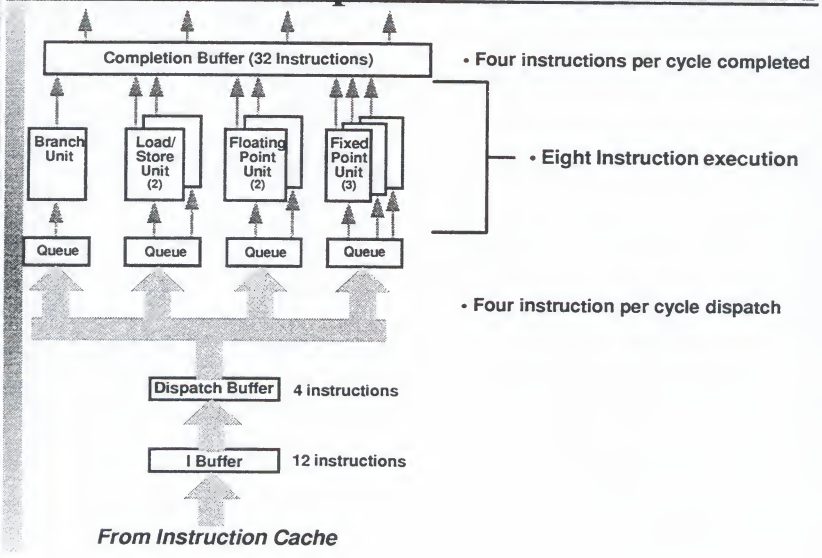
- 32KB instruction cache
  - 128-way associativity
  - 128-byte line size
  - 2-way interleaved

High Bandwidth: *Data Cache*

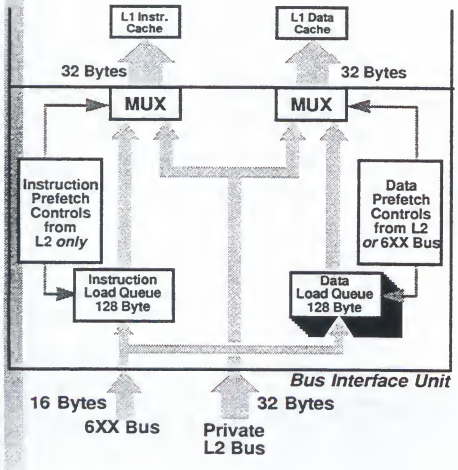


- 64KB data cache
  - 128-way set associative
  - 8-way interleaved
    - 4-way by line
    - 2-way by double word

Decode-to-Completion Bandwidth



Reduced Latency Memory Subsystem



- Non-blocking caches
  - Four outstanding data L1 demand requests
  - Two outstanding instruction L1 demand requests
- Dedicated hardware prefetch to L1, L2 and main memory
  - I-side prefetch to predicted path and next line
  - D-side prefetch to up to four streams, each stream prefetches next two lines

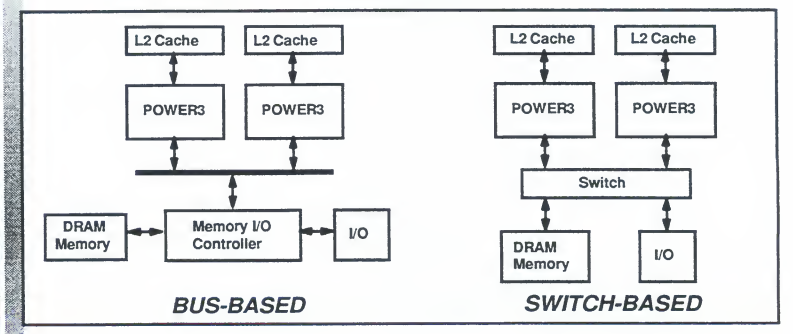
Verification

IBM

- Challenge
  - Verify a highly superscalar design in multiple system configurations
- Methodology
  - Simulation used over 400 POWER2-class RS/6000 systems
  - 90 billion cycles targeted to cover
    - Over 100,000 defined logic events
    - Over 10,000 memory hierarchy bus scenarios
  - Thousands of checks executed on every cycle of testing
  - Majority of testing targeted to MP
  - Extensive array switch level simulation
- Results
  - Booted OS environment on first pass silicon
  - Achieved MP functionality on first pass silicon

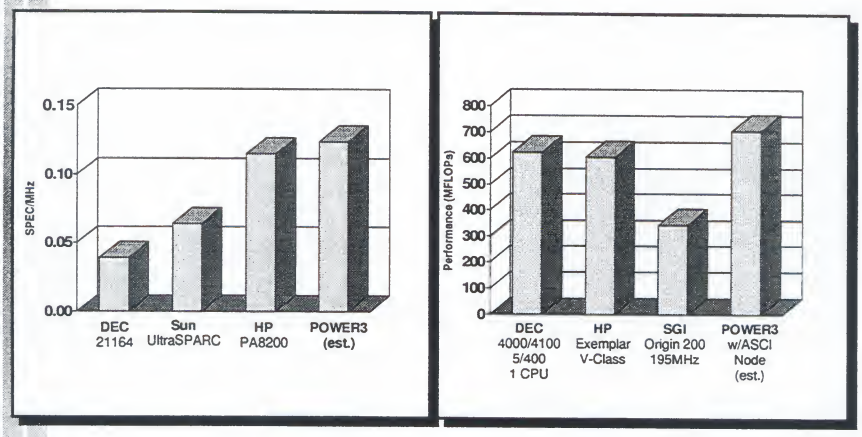
System Implementation

IBM



- Supports bus- and switch-based MP bus memory configurations

Performance



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Rev the Engine...

- POWER3 processor in system bring-up phase
  - First pass silicon 1Q97
  - Initial design center 200+ MHz achieved
- Design focus to bring POWER3 to leading-edge technology and tune architecture
  - Implementation in CMOS 7S
  - 0.20 micron technology
  - Copper metallurgy
- Design honed for higher clock speed and commercial application performance
  - Set associative L2 support
  - Fractional bus modes
- Next POWER3 processors in design phase
  - 300+ MHz and 500+ MHz design targets

Summary

IBM

- Very robust design point...
  - *High bandwidth*
  - *Highly superscalar*
  - ...to match customer's requirement for high computational capability
- Functionality on first pass silicon
- Two follow-on POWER3 design efforts underway

PA-8500: Scaling the PA-8200 with a Large Integrated Cache

Bill Queen, *Hewlett-Packard*

presented by MICRODESIGN RESOURCES

The HP PA-8500 RISC CPU

High Speed SRAM with an Integrated CPU

Bill Queen
Systems Technology Division
Hewlett-Packard Company

HEWLETT PACKARD

Presentation Overview

PA-RISC POWERED

- Cache SRAM Trends
- Goals of the PA-8500
- PA-8500 Processor Core
- Improvements
- Caches
- System Bus

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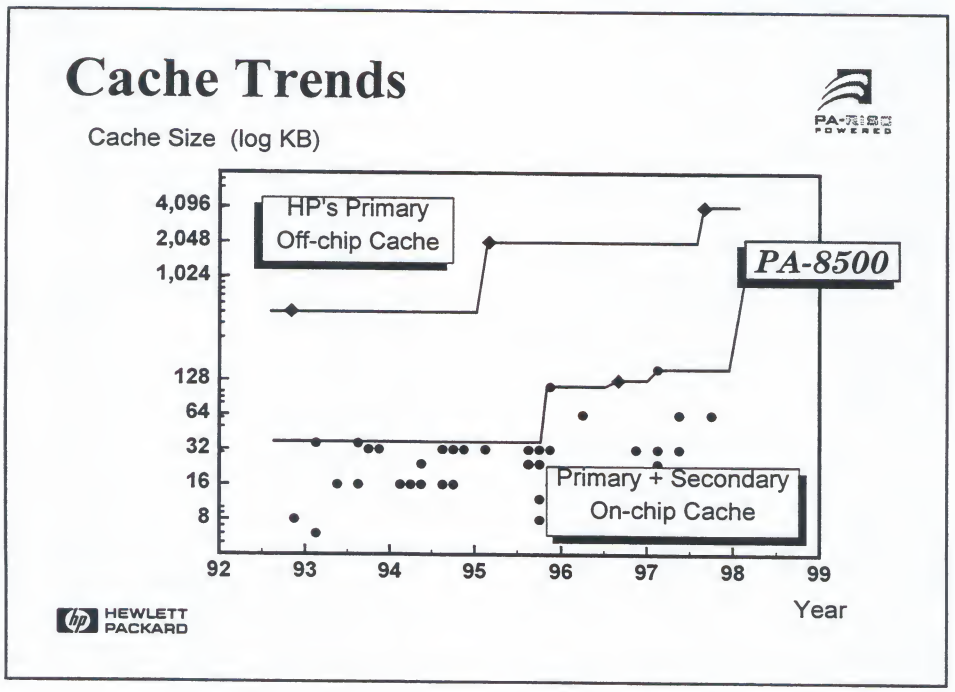


Goals for the PA-8500

PA-RISC POWERED

- Leadership application performance
- Reduced system cost
- Full performance without recompilation on PA-8x00 binaries

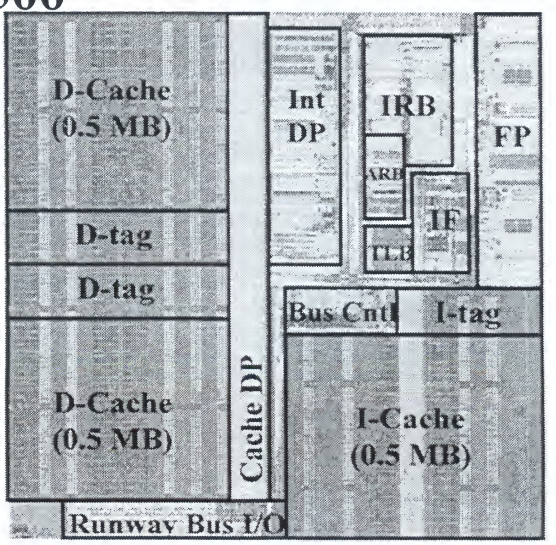
HEWLETT PACKARD

PA-8500 Strategy

- Boost frequency by porting to 0.25 micron
- Design aggressive fast and large primary cache
- Combine cache and CPU on one die
- Increase bandwidth to main memory

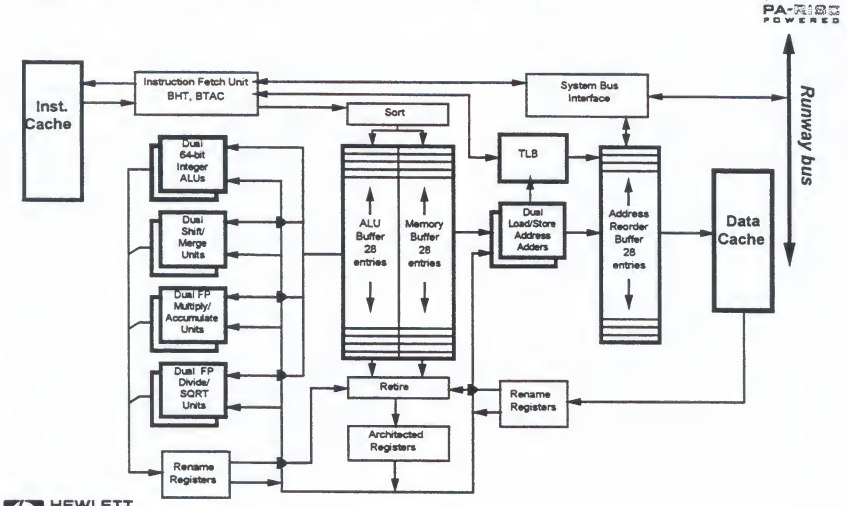
HEWLETT PACKARD

PA-8500



HEWLETT PACKARD

PA-8500 Processor Core



HEWLETT PACKARD

Key Improvements to Processor Core

- Larger 160-entry TLB
- Larger 2048-entry BHT
- Improved branch prediction ("agrees" mode)

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PA-8500 Branch Prediction Modes

- Static — Compiler-directed (Heuristics/PBO)
- Dynamic — Hardware-directed ("Taken/Not taken")
- "Agrees" — Dynamic prediction using static hints

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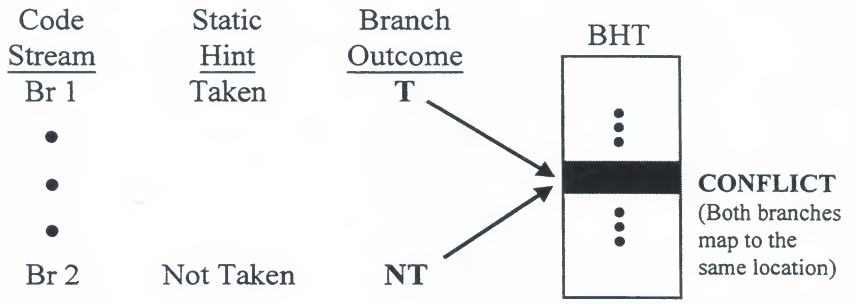
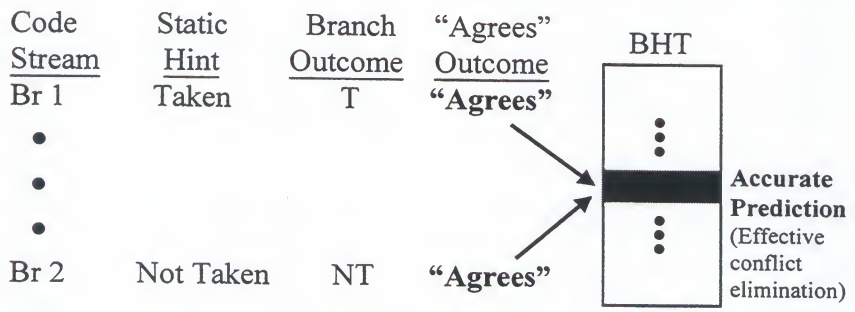
Dynamic Prediction: Problem



Conflict in the BHT causes poor branch prediction and degrades performance

HEWLETT PACKARD

Dynamic Prediction: Solution



"Agrees" Mode

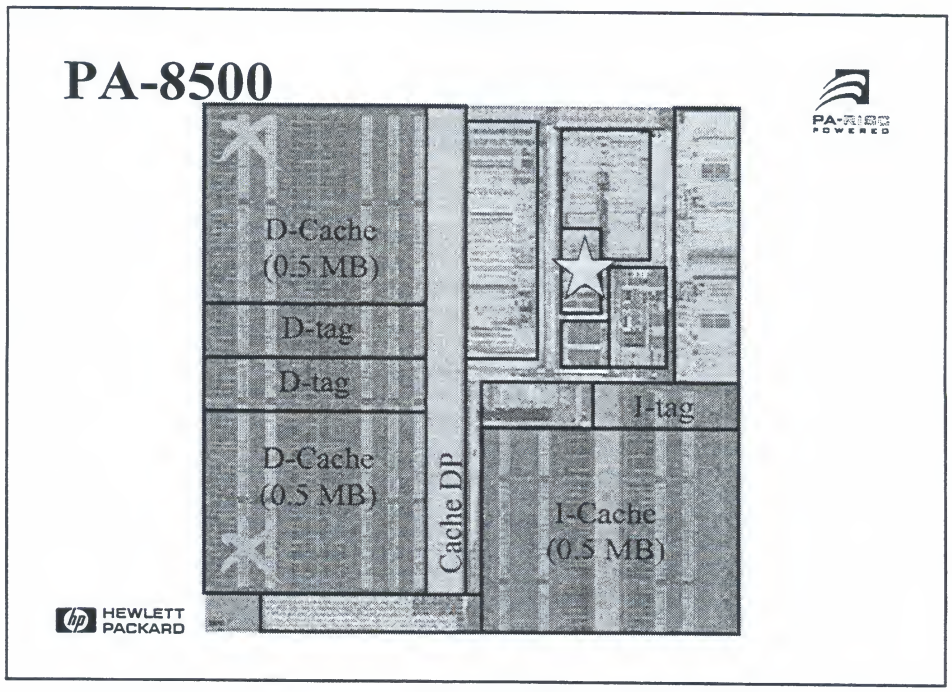
Improves performance by increasing branch prediction accuracy
Effectively results in a larger number of BHT entries

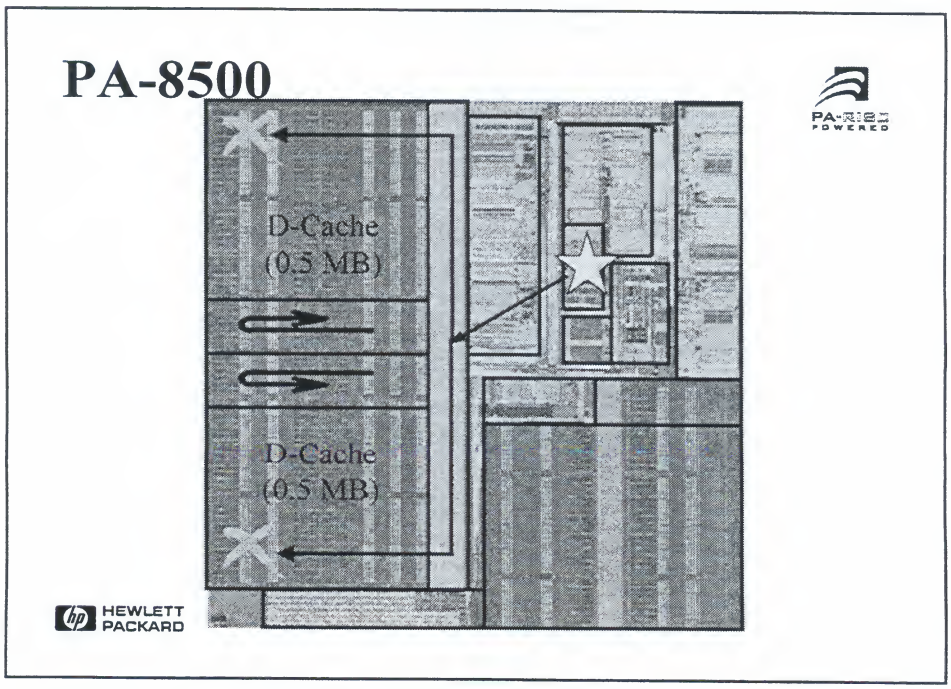
HEWLETT PACKARD

PA-8500 Caches

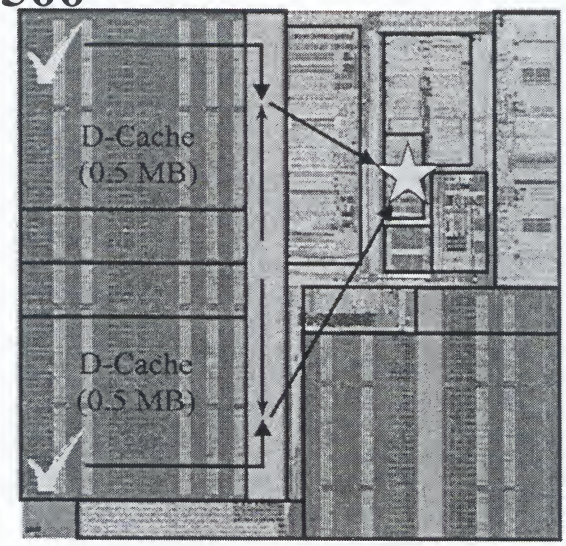
Data Cache	1.0 MB 4-way set associative
Instruction Cache	0.5 MB 4-way set associative
Frequency	360+ MHz
Latency	2-cycle pipelined access
Bandwidth	2 accesses/cycle
Cache-Line Support	32-byte
	64-byte
Error Protection	Single-bit-correct ECC

HEWLETT PACKARD


PA-8500
D-Cache
(0.5 MB)
D-tag
D-tag
D-Cache
(0.5 MB)
Cache DP
I-tag
I-Cache
(0.5 MB)
HEWLETT
PACKARD


PA-8500
D-Cache
(0.5 MB)
D-Cache
(0.5 MB)
HEWLETT
PACKARD

PA-8500



HEWLETT PACKARD

Large Fast Caches

Design Solutions

- Careful composition (e.g. associativity)
- Effective use of silicon resources
- Cancel effects of clock skew
- Special cache clocks
- Special attention to the functional definition

HEWLETT PACKARD

PA-8500 Caches

- Unprecedented design:
  High bandwidth, low latency, and large size !
- Balanced CPU execution bandwidth
- Simplicity of solution

PA-8500 System Bus

- Higher bandwidth mode
  - 2X increase in bandwidth
  - 1 state for address + 2 data transfers per state
  - 64B line-size
- Designed to enable higher bus frequencies

PA-8500: Meeting the Needs of a Diverse Product Line

- High-performance processor core
- Integrated SRAM and CPU
- Supports a variety of system configurations

A SPARC Microprocessor for High-End Servers

Hisashige Ando,
HAL Computer Systems

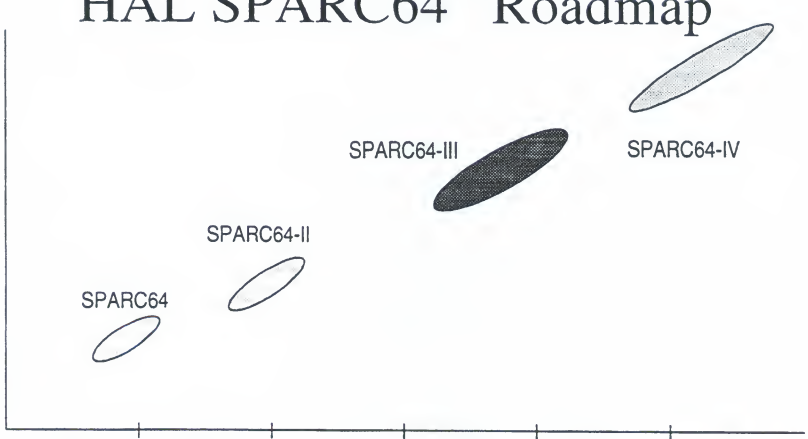
presented by MICRODESIGN RESOURCES

A SPARC Microprocessor for High-End Servers – SPARC64™-III –

Hisashige Ando
HAL Computer Systems Inc.

Microprocessor Forum
October 14, 1997

HAL SPARC64™ Roadmap

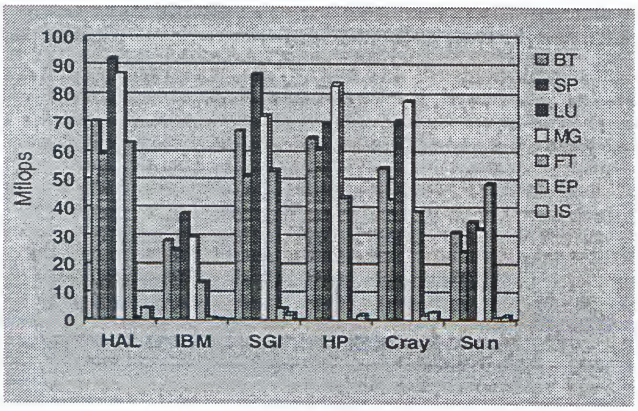


HALstation™ 385

- Powered by SPARC64-II CPU
- 161MHz Clock
- 9.0 SPECint95 (peak)
- 16.0 SPECfp95 (peak)
- Mainly used for Compute Server
  - Scientific and R&D
  - EDA

HALstation™ 385

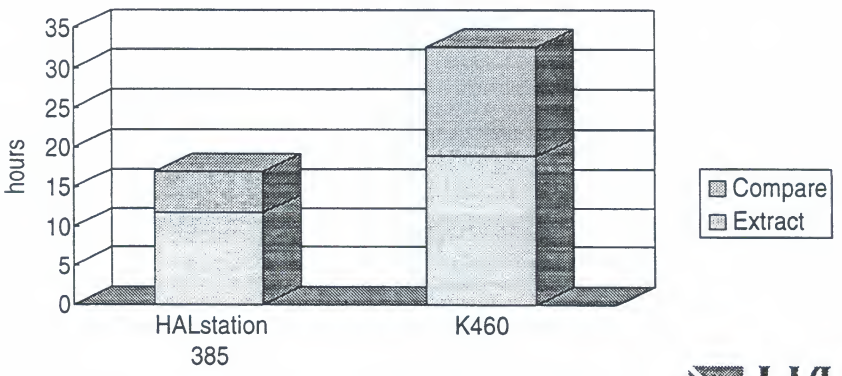
NASPAR2.2 Class A Benchmark Results



HALstation 385 (161 MHz)
IBM P2SC (120MHz)
SGI Origin 2000
HP SPP2000
CRAY T3e-900 (450MHz)
Sun Ultra 4000

HALstation™ 385

Calibre LVS Run time for SPARC64-III chip



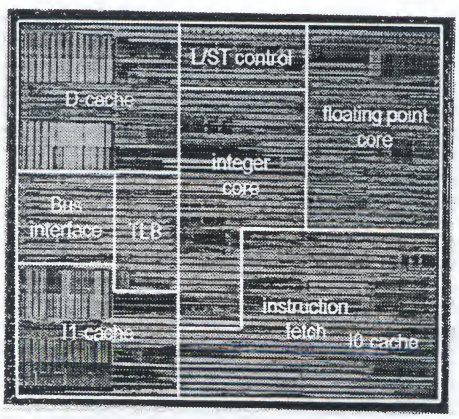
SPARC64™-III Key features

- SPARC V9, 64bit, 4 issue superscalar, out-of-order execution processor
- Full 64-bit virtual address support and large TLB for large memory applications
- On-chip L2 cache controller supports 1M-16MB external L2 cache
- UPA-compatible system bus interface
- ECC & Parity protection for high reliability

SPARC64™-III Physical features

- 17.6M transistors
- 15.98 x 14.85 mm chip
- 0.25um CMOS technology
  - Transistor: L_{eff}= 0.18µm , t_{ox}=5.5nm
  - 5 layer Metal + LI
  - 0.9um/0.9um/0.9um/1.8um/2.7um pitch
- Flip Chip
- 957 pin Land Grid Array package

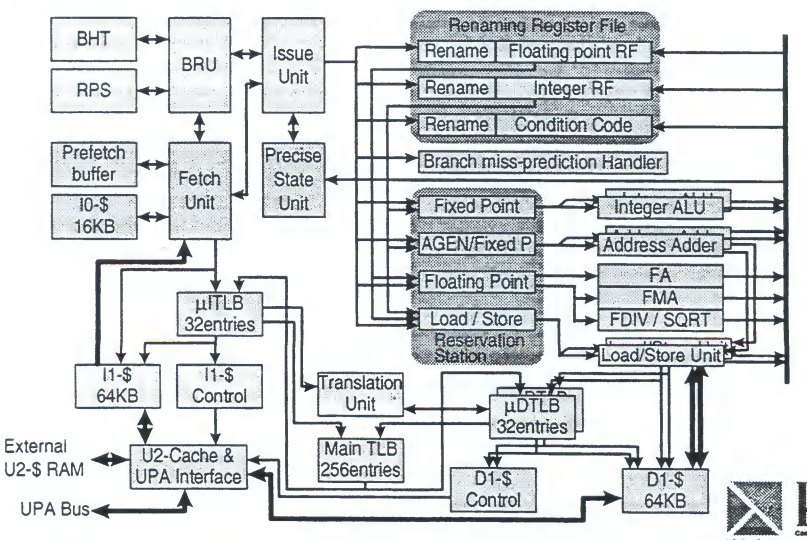
SPARC64™-III Die photo



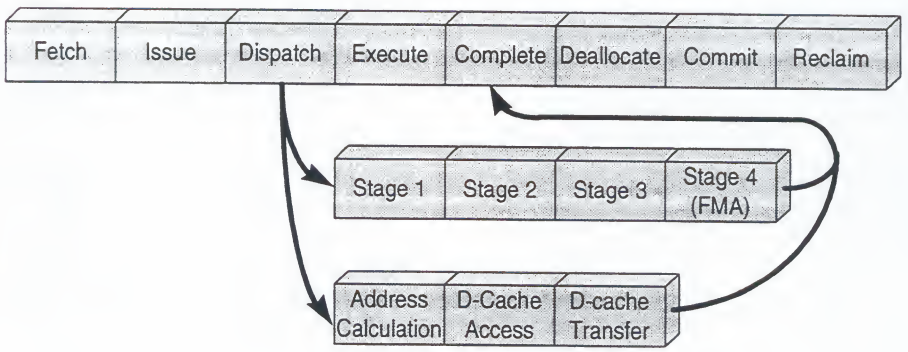
SPARC64™-III Microarchitecture

- 4 instruction issue per cycle
- Reservation Stations: 8 entries for integer, agen, and floating point execution units, 12 entries for ld/st address queue
- 6 operation dispatch per cycle: 2 integer, 2 agen, 2 floating point
- Renaming Register file
- Separate µTLB and large (unified) TLB
- 2 bank, 2 access/cycle D-Cache

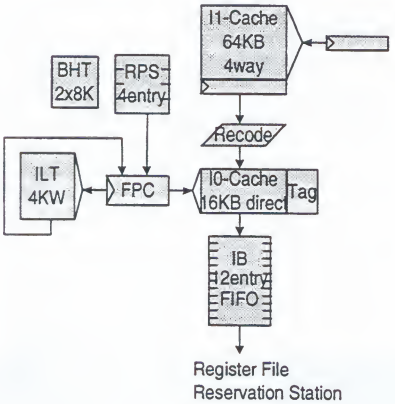
SPARC64™-III Block Diagram



SPARC64™-III Pipeline

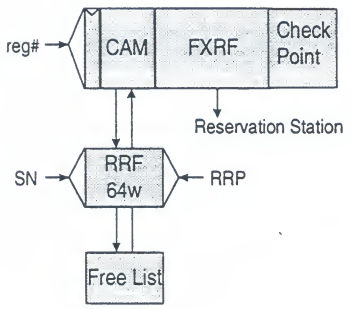


SPARC64™-III Fetch and Issue unit



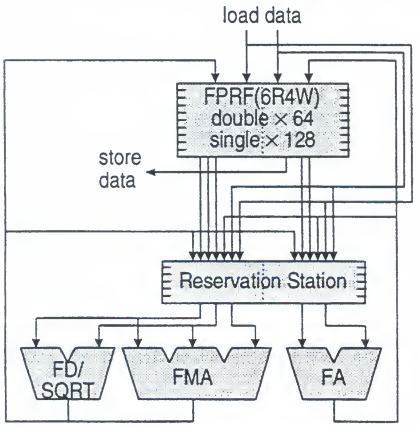
- ILT (instruction link table): Predict next fetch PC
- BHT (branch history table): Supports both One and Two level adaptive / 2-bit counter
- RPS (return prediction stack)
- I0-Cache: level 0 recoded instruction cache

SPARC64™-III Renaming Reg file



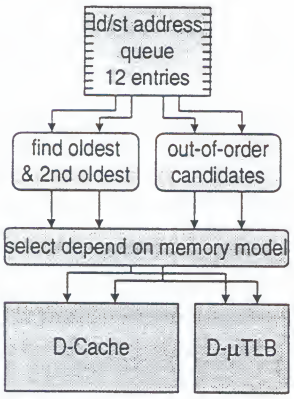
- integer:
  - 5 windows
  - 128 words
  - 10 read / 4 write
  - 16 check points
- floating point:
  - 64 double precision or 128 single precision entries
  - 6 read / 4 write
  - 16 check points

SPARC64™-III
Floating Point execution unit



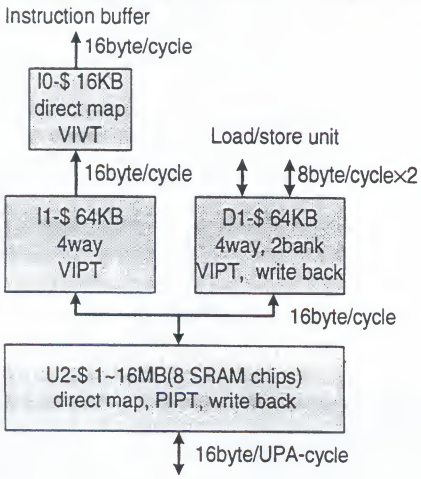
- multiply and add
  - 4 cycle latency
  - 1 cycle pitch pipelined
- add
  - 3 cycle latency
  - 1 cycle pitch pipelined
- divide / square root
  - 12 cycle (single)
    21 ~ 22 cycle (double)
    latency

SPARC64™-III Load/Store Unit



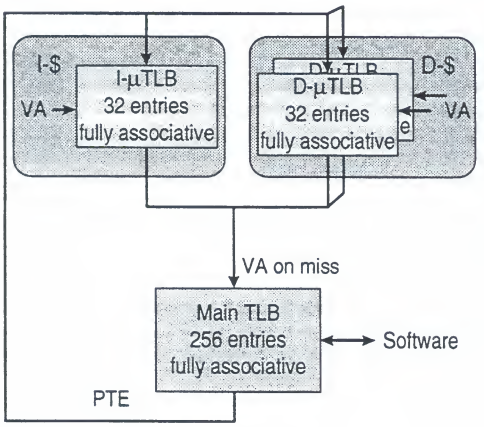
- 2 load/store operations per cycle
- support 3 memory models
  - LSO: load store ordering
  - TSO: total store ordering
  - STO: store ordering

SPARC64™-III Cache hierarchy



- I0-$: recoded instruction cache
- On chip 64KB + 64KB separate cache
- Off chip large unified cache support

SPARC64™-III Address Translation Hierarchy



- variable page sizes (16): 4KB to 4GB
- OS and DB SGA can be mapped with few giant pages
- 2 level TLB: fast access and large capacity

SPARC64™-III Summary

- Carries HAL SPARC64™ architecture into future
  - Full 64bit architecture and implementation
  - >50% faster than current SPARC64™-II
- For computational server and database server
  - Large Memory Support
  - High reliability with ECC & parity
- Single Chip CPU
  - 1~16MB off chip L2 cache support
  - integrated UPA interface

MICROPROCESSOR FORUM 97

www.MDRonline.com/mpf

TENTH ANNIVERSARY

PANEL

Maximizing RISC Microprocessor Performance

Linley Gwennap, *moderator, Microprocessor Report*
Gary Lauterbach, *Sun Microsystems*
Mark Papermaster, *IBM*
Bill Queen, *Hewlett-Packard*
Hisashige Ando, *HAL Computer Systems*
Earl Killian, *MIPS*
Dan Leibholz, *Digital Semiconductor*

presented by MICRODESIGN RESOURCES

The E4 MPEG-2 Video Codec

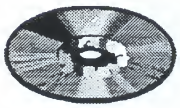
Les Kohn, *C-Cube Microsystems*

presented by MICRODESIGN RESOURCES

DVx MPEG-2 Video Codec

C-Cube Microsystems

Fulfilling the Promise of Digital Video

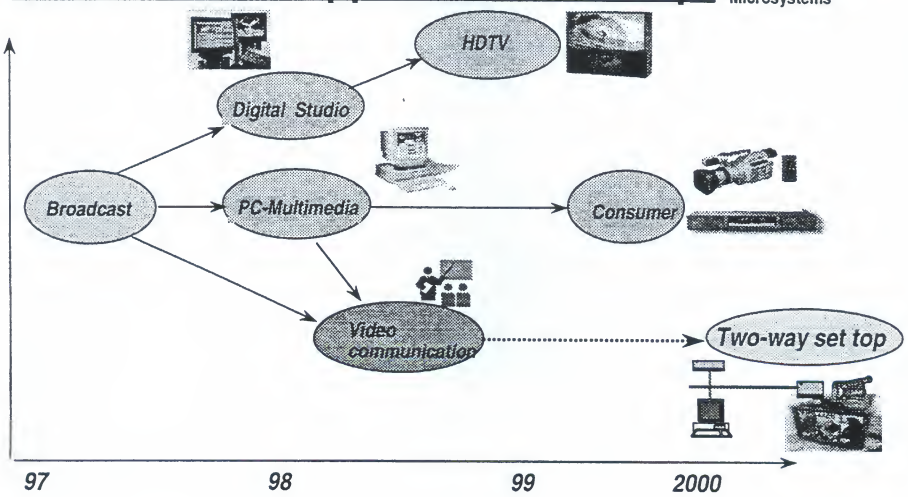


Les Kohn
C-Cube Microsystems

1

MPEG Encode Application Roadmap

C-Cube Microsystems



2

DVx Objectives

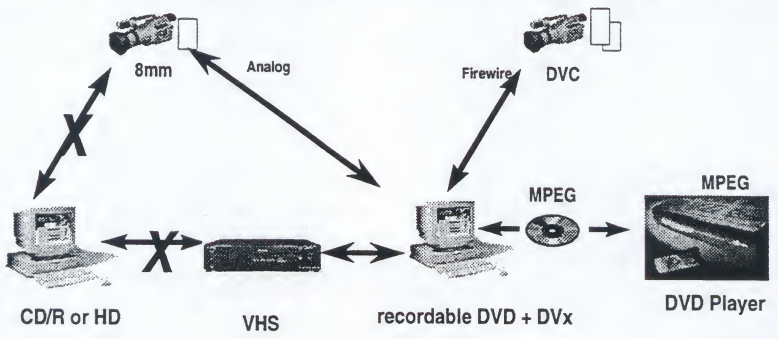
C-Cube Microsystems

- Enable MPEG-2 content creation on PC
- Low delay simultaneous encode and decode for video communication
- Professional profile for studio applications
- Scaleable to HDTV
- State of art quality

3

DVx: The Path to Personal Publishing

C-Cube Microsystems



Incompatible recording & playback formats

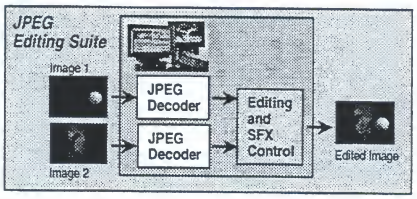
Compatible disc-based PC recording and DVD Playback

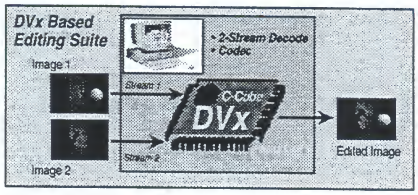
4

DVx Enables MPEG-2 Video Editing

C-Cube Microsystems

- ▼ Dual Stream Decode with Effects
  - ✔ Frame Accurate Non Linear Editing
- ▼ Advantages of MPEG-2
  - ✔ Compatibility with DVD & DVB
  - ✔ Storage and Bandwidth Savings
    - ◆ JPEG = 30 - 50 mbps
    - ◆ MPEG-2 = 4 - 18 mbps

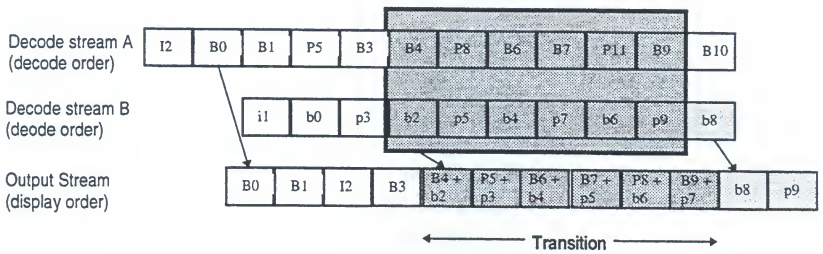




5

Dual Stream Editing Example

C-Cube Microsystems



6

Design Concepts

C-Cube Microsystems

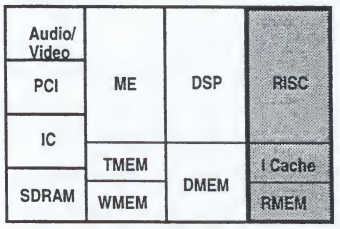
- **Standard RISC engine for High Level Operations**
  - ✔ Flexibility to support different applications and add features
  - ✔ Ease of programming and good tools
  - ✔ Quick bug fixing
- **CISC Coprocessors for Pixel Operations**
  - ✔ Optimized hardware for performance critical functions
  - ✔ Complex instructions minimize risc core demands
- **Design for Worst Case, not Average Performance**
  - ✔ Avoid cache, main memory and vlc bottlenecks

7

RISC Engine

C-Cube Microsystems

- **MicroSPARC 32-bit RISC**
  - ✔ Single Scalar
  - ✔ Fast simulation w/Sparc WS
- **16K byte Instruction Cache**
  - ✔ No misses inside of loops
- **8K byte Data Memory**
  - ✔ Software Managed
  - ✔ Overlapped DMA transfers
  - ✔ Predictable performance, unlike Cache
    - ◆ Cache misses would be unavoidable inside loops

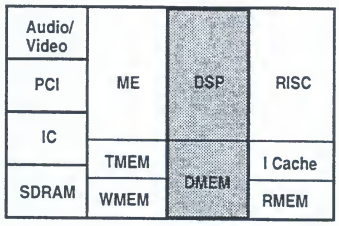


8

DSP Coprocessor

C-Cube Microsystems

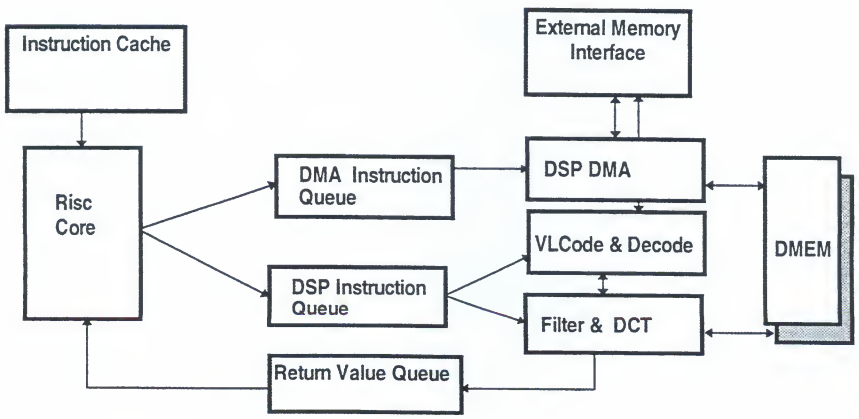
- ▼ Vector M->M instructions
  - ✔ Sparc Coprocessor Instructions
  - ✔ Code density and low issue rate
- ▼ 8Kx8 Data Memory
  - ✔ Double buffered to allow concurrent DMA and DSP
- ▼ DSP Functions
  - ✔ DeTelecine
  - ✔ Activity Measures
  - ✔ Motion Compensation
  - ✔ Adaptive Temporal Filter
  - ✔ Linear Filter / Decimation
  - ✔ DCT/IDCT
  - ✔ Quantization / Dequantization
  - ✔ Variable Length Coding / Decoding



9

DSP Instruction Execution

C-Cube Microsystems



10

DSP Synchronization

C-Cube Microsystems

Instructions:

- ✔ Swapdsp
- ✔ Syncdsp
- ✔ Syncrmem

To Process N blocks of data:

- ✔ Do for n + 2 iterations:
  - ◆ If not last two iterations perform DMA DSP loads
  - ◆ If not first or last iteration perform DSP operations
  - ◆ If not first two iterations perform DSP stores
  - ◆ swapdsp

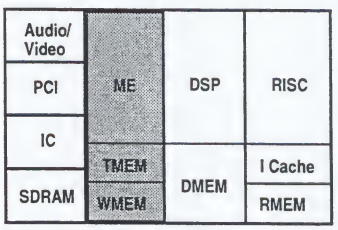
11

ME Coprocessor

C-Cube Microsystems

▼ **Architecture**

- ✔ Doubled buffered Target and Reference Memories
- ✔ Reuse data between targets
- ✔ 64 abs diff/cycle throughput



▼ **Programmable ME Algorithm with Minimal Risc Core Overhead**

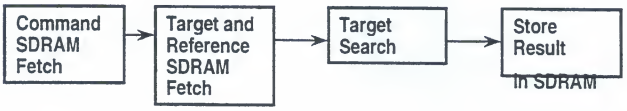
- ✔ RISC CPU writes ME search command for each target in sdram
- ✔ ME writes search result list in sdram
- ✔ Single interrupt generated at end of each ME stage

12

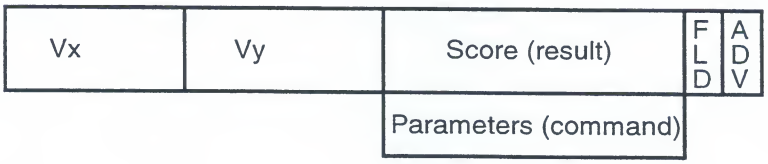
ME Command Processing

C-Cube Microsystems

▼ ME Pipeline



▼ ME Command and Result Format

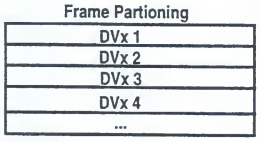


13

Inter-chip Communication

C-Cube Microsystems

▼ Scaleable to HDTV
- ✔ Image reference data transfers
- ✔ Master/slave control



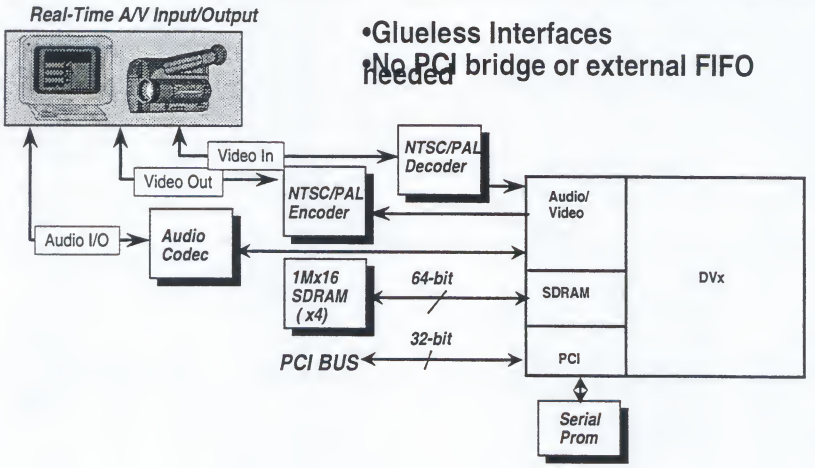
▼ Independent Receive /Transmit Channels (2 each)

▼ Simple Protocol
- ✔ Packet based
- ✔ Routing to appropriate chip based on address field in header

14

DVx System Configuration

C-Cube Microsystems



15

DVx Statistics

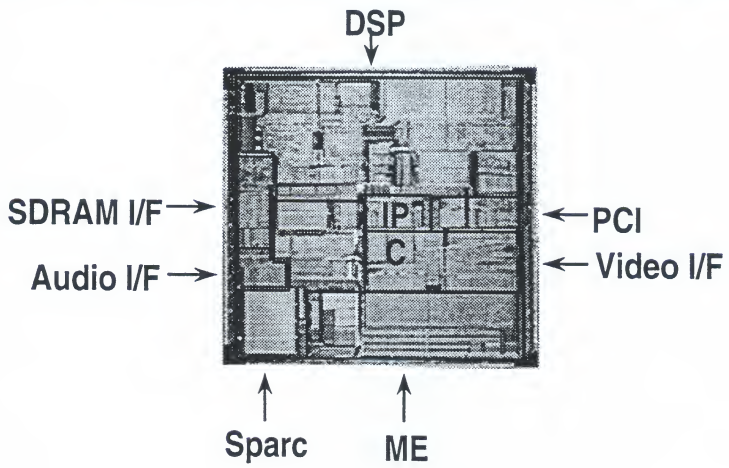
C-Cube Microsystems

- 5.4 Million Transistors
- 100-MHz
- 162 sq mm
- .35µ 4LM CMOS
- 4.7W @ 3.3V (encode)
- 352 pin BGA
- Sampling now, production 12/97

16

DVx Die Photo

C-Cube Microsystems

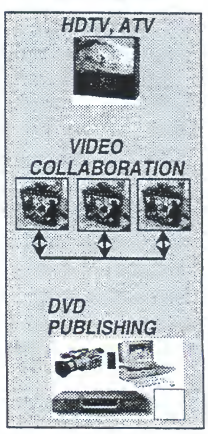


17

Summary

C-Cube Microsystems

- Cost Effective, Multi-Application Codec
- Flexible: Programmable and Scaleable
- Professional
  - Enables migration to HDTV, ATV
  - Video Collaboration
- Prosumer - DVx + Recordable DVD
  - Complete mpeg-2 content creation solution
  - Broadcast quality at entry level price



DVx : Fulfilling the Digital Video Promise

18

ManArray Technology: The Scalable Future of Signal Processing

Gerald Pechanek, *BOPS*

presented by MICRODESIGN RESOURCES

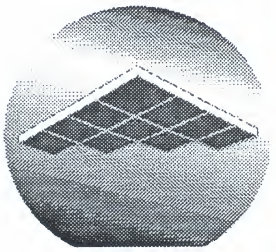
Billions of Operations Per Second

Presents for the first time

ManArray™ Technology:

The Scalable Future of Signal Processing

by Gerald G. Pechanek, CTO.



BOPS
INCORPORATED
...a chipless chip company.

Representing the
ManArray Design Team
Chapel Hill, North Carolina.

BOPS
INCORPORATED

ManArray™

- A scalable architecture for a family of high-performance single-chip parallel processors
- Based on a compute array of Processing Elements (PEs) and controller Sequence Processors (SPs)
- Billion-operations-per-second performance in 3D graphics, video compression, audio, and other compute-intensive tasks

Page 2

BOPS INCORPORATED

The ManArray™ Technology Message

fast **ManArray™ Delivers Performance**
- Optimized scalar, packed data, eVLIW, Vector, SIMD, & Multiple-SIMD
- Single cycle PE-to-PE communications through novel ManArray network

scalable **ManArray™ Scales to Multiple Products**
- Family of high performance cores: 1x1, 1x2, 2x2, 2x4, 4x4, 4x4x4
- Novel interconnection network between PEs and clusters of PEs
- Software investment scales across core family

programmable **ManArray™ Is Easy & Fun to Program**
- Open instruction set architecture & tool set across BOPS products
- Selectable parallel programming models: DSP, eVLIW, vector, SIMD

low cost **ManArray™ Is Low-Cost & License-able**
- Novel ManArray topology & eVLIW design reduces chip wiring
- Regular layout lowers cost and increases performance

Page 3

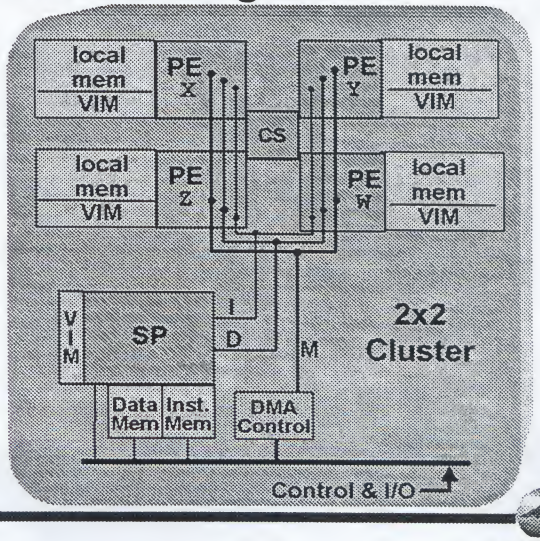
BOPS INCORPORATED ManArray™ fast scalable programmable low cost

2x2 Cluster Building Block:

Logic Core:
Processor Elements (PEs)
Cluster Switch (CS)
Sequence Processor (SP)

Application-sized Memory:
PE Local Data Memory
SP Data Memory
SP Instruction Memory
VLIW Memory (VIM)

Buses & Control:
bandwidth matched to topology
Instruction Bus (I)
Data Bus (D)
DMA Bus (M)
Control & I/O Bus
DMA Controller



Page 4

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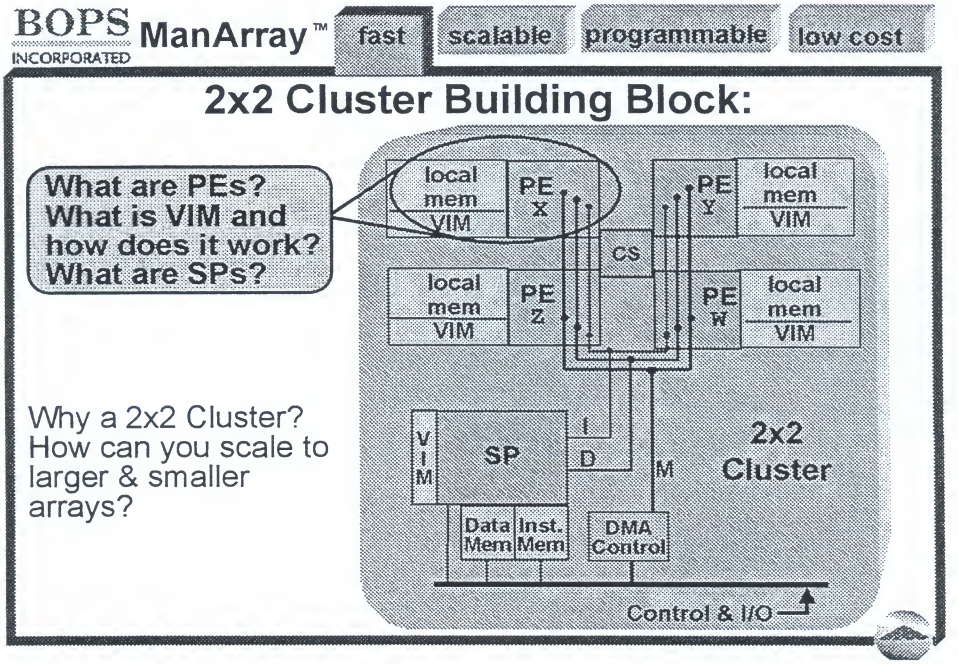
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
2x2 Cluster Building Block:
What are PEs?
What is VIM and how does it work?
What are SPs?
Why a 2x2 Cluster?
How can you scale to larger & smaller arrays?
local mem VIM
PE X
PE Y
PE Z
PE W
CS
SP
I
D
M
2x2 Cluster
Data Mem
Inst. Mem
DMA Control
Control & I/O
Page 5
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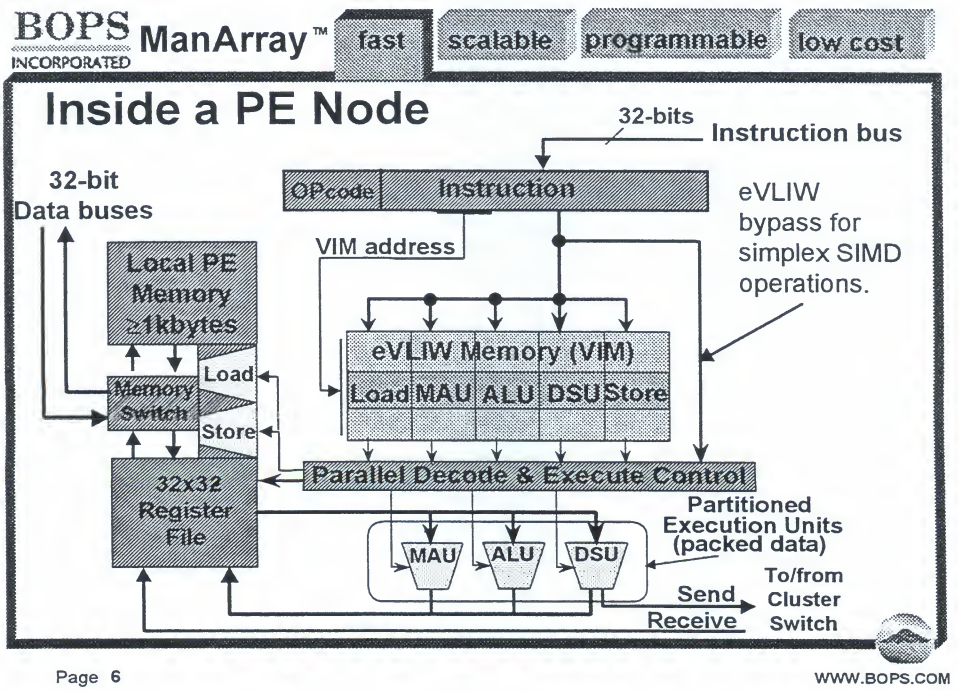
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
Inside a PE Node
32-bits
Instruction bus
32-bit Data buses
OPcode
Instruction
VIM address
eVLIW bypass for simplex SIMD operations.
Local PE Memory ≥1kbytes
Memory Switch
Load
Store
eVLIW Memory (VIM)
Load
MAU
ALU
DSU
Store
32x32 Register File
Parallel Decode & Execute Control
Partitioned Execution Units (packed data)
MAU
ALU
DSU
Send
Receive
To/from Cluster Switch
Page 6
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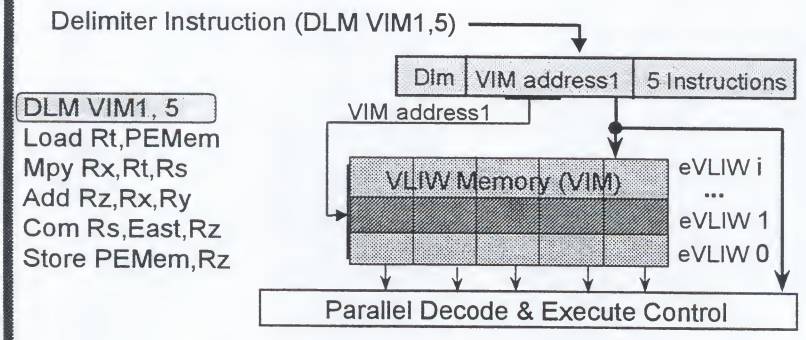
eVLIW Setup



The Delimiter Instruction sets the VIM address pointer.

An eVLIW is an encapsulated set of 32-bit instructions located at a specified VIM address.

Page 7

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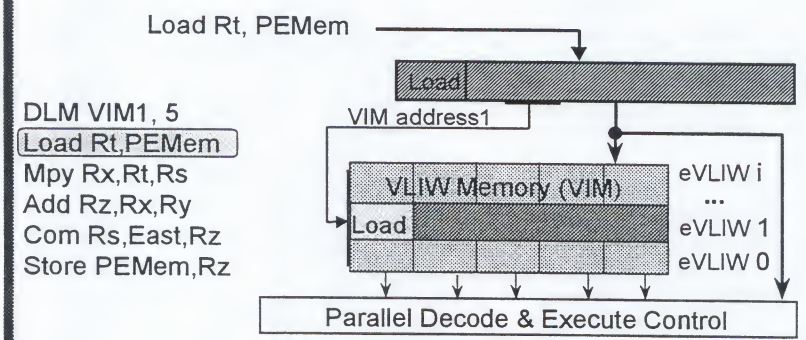
eVLIW Flow



Page 8

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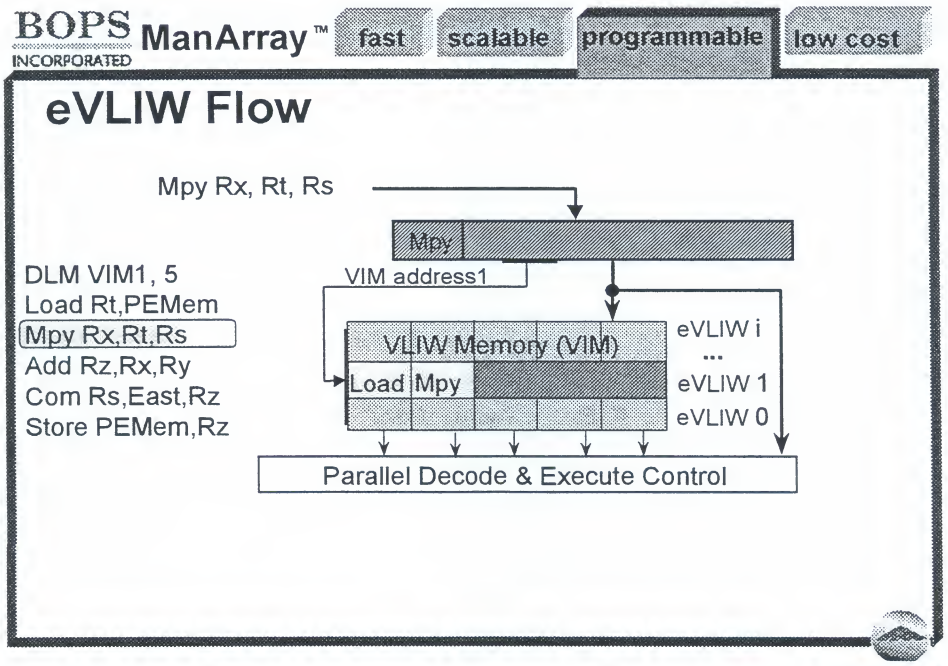
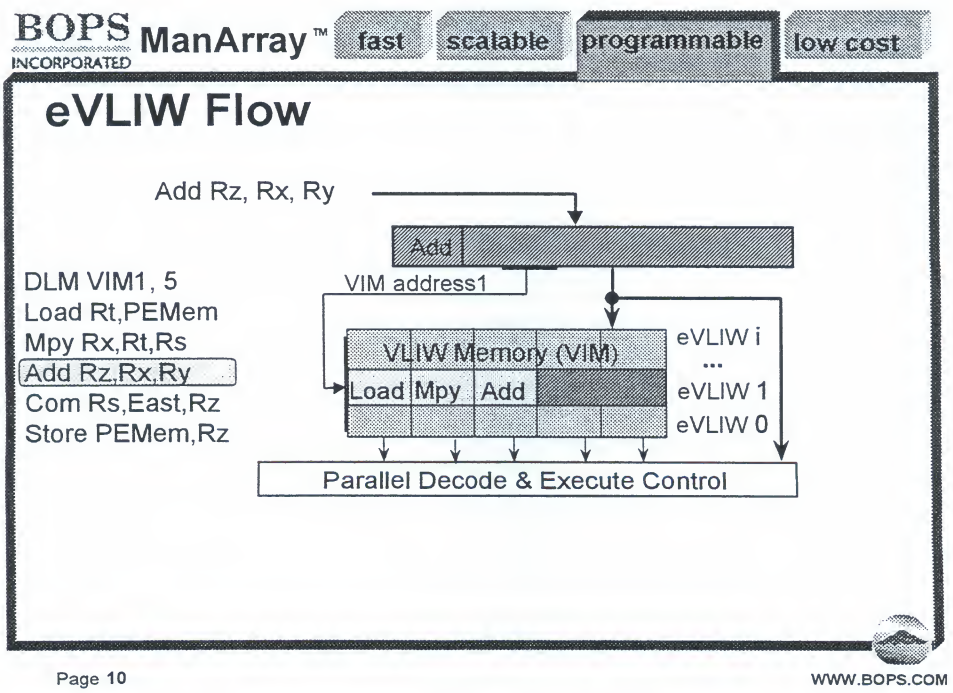

BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
eVLIW Flow
Mpy Rx, Rt, Rs
Mpy
VIM address1
DLM VIM1, 5
Load Rt,PEMem
Mpy Rx,Rt,Rs
Add Rz,Rx,Ry
Com Rs,East,Rz
Store PEMem,Rz
VLIW Memory (VIM)
Load Mpy
eVLIW i
...
eVLIW 1
eVLIW 0
Parallel Decode & Execute Control
Page 9
WWW.BOPS.COM


BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
eVLIW Flow
Add Rz, Rx, Ry
Add
VIM address1
DLM VIM1, 5
Load Rt,PEMem
Mpy Rx,Rt,Rs
Add Rz,Rx,Ry
Com Rs,East,Rz
Store PEMem,Rz
VLIW Memory (VIM)
Load Mpy Add
eVLIW i
...
eVLIW 1
eVLIW 0
Parallel Decode & Execute Control
Page 10
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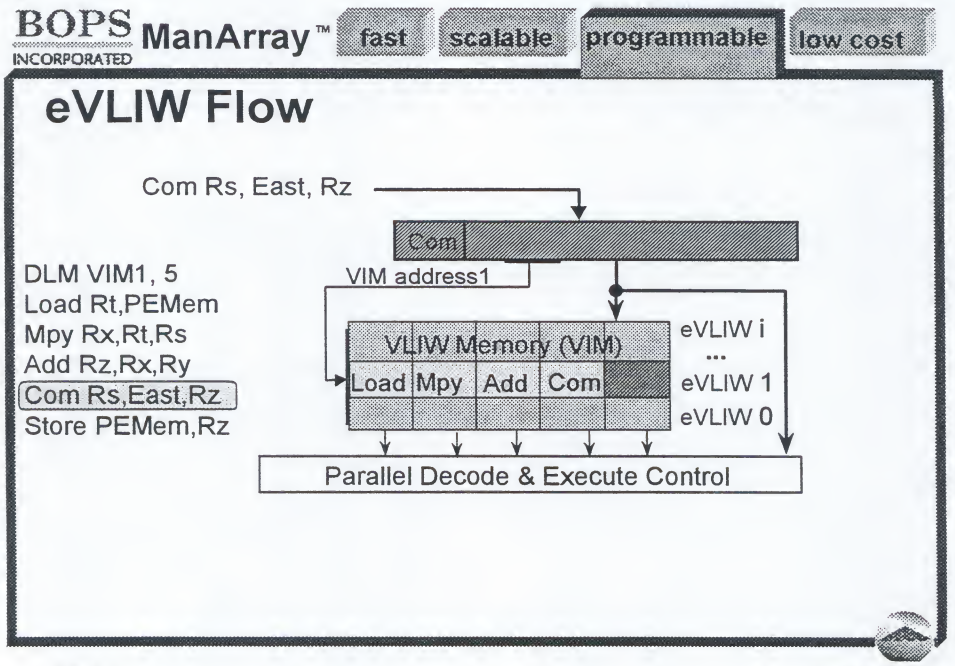
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
eVLIW Flow
Com Rs, East, Rz
Com
DLM VIM1, 5
Load Rt,PEMem
Mpy Rx,Rt,Rs
Add Rz,Rx,Ry
Com Rs,East,Rz
Store PEMem,Rz
VIM address1
VLIW Memory (VIM)
Load Mpy Add Com
eVLIW i
...
eVLIW 1
eVLIW 0
Parallel Decode & Execute Control
Page 11
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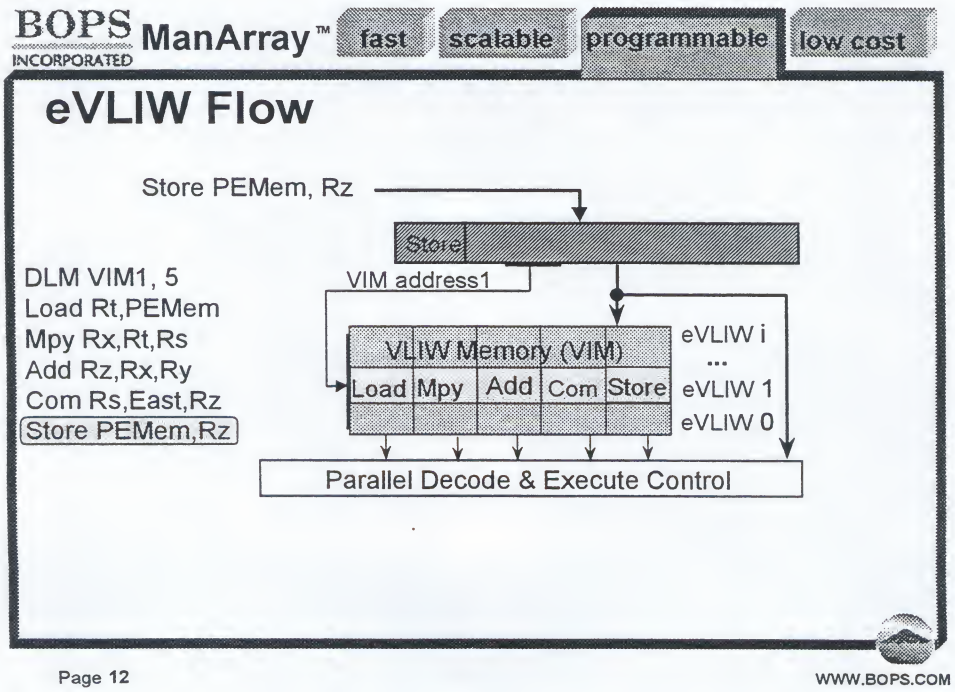
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
eVLIW Flow
Store PEMem, Rz
Store
DLM VIM1, 5
Load Rt,PEMem
Mpy Rx,Rt,Rs
Add Rz,Rx,Ry
Com Rs,East,Rz
Store PEMem,Rz
VIM address1
VLIW Memory (VIM)
Load Mpy Add Com Store
eVLIW i
...
eVLIW 1
eVLIW 0
Parallel Decode & Execute Control
Page 12
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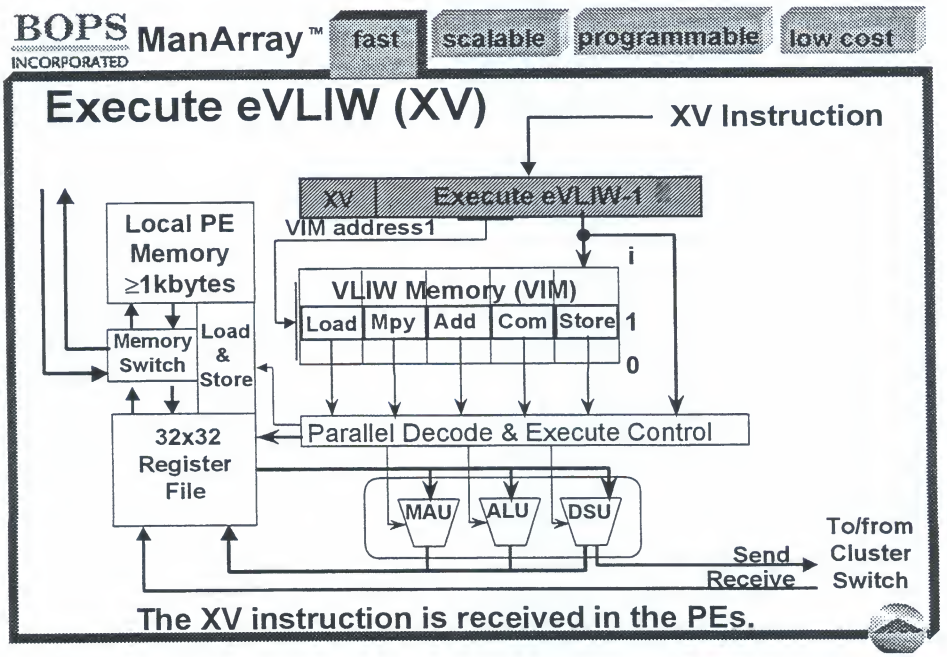
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
Execute eVLIW (XV)
XV Instruction
XV
Execute eVLIW-1
VIM address1
i
Local PE Memory ≥1kbytes
VLIW Memory (VIM)
Load
Mpy
Add
Com
Store
1
0
Memory Switch
Load & Store
32x32 Register File
Parallel Decode & Execute Control
MAU
ALU
DSU
To/from Cluster Switch
Send
Receive
The XV instruction is received in the PEs.
Page 13
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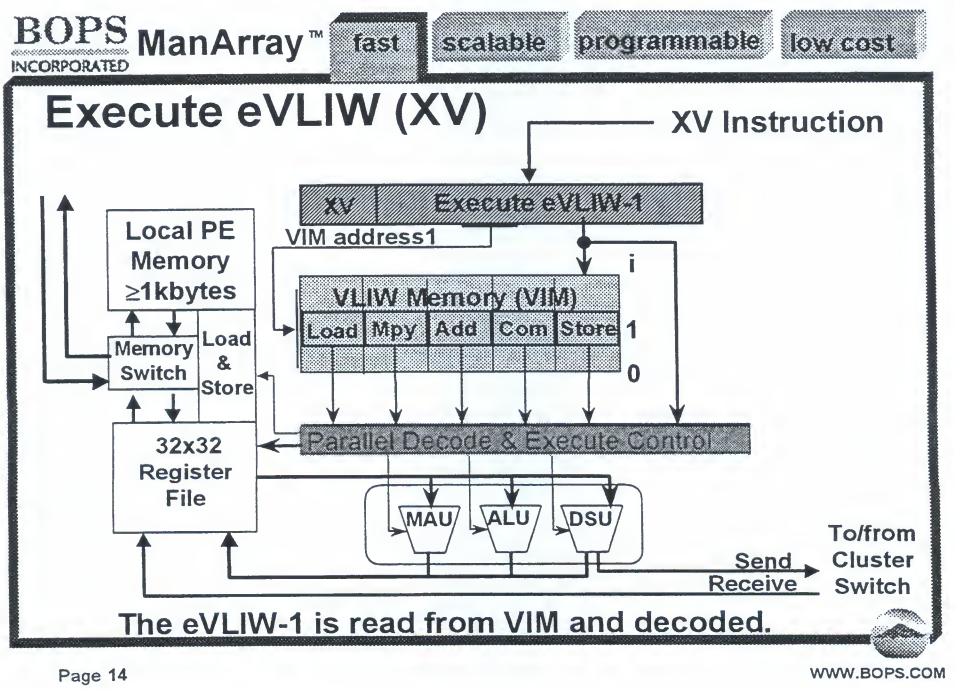
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
Execute eVLIW (XV)
XV Instruction
XV
Execute eVLIW-1
VIM address1
i
Local PE Memory ≥1kbytes
VLIW Memory (VIM)
Load
Mpy
Add
Com
Store
1
0
Memory Switch
Load & Store
32x32 Register File
Parallel Decode & Execute Control
MAU
ALU
DSU
To/from Cluster Switch
Send
Receive
The eVLIW-1 is read from VIM and decoded.
Page 14
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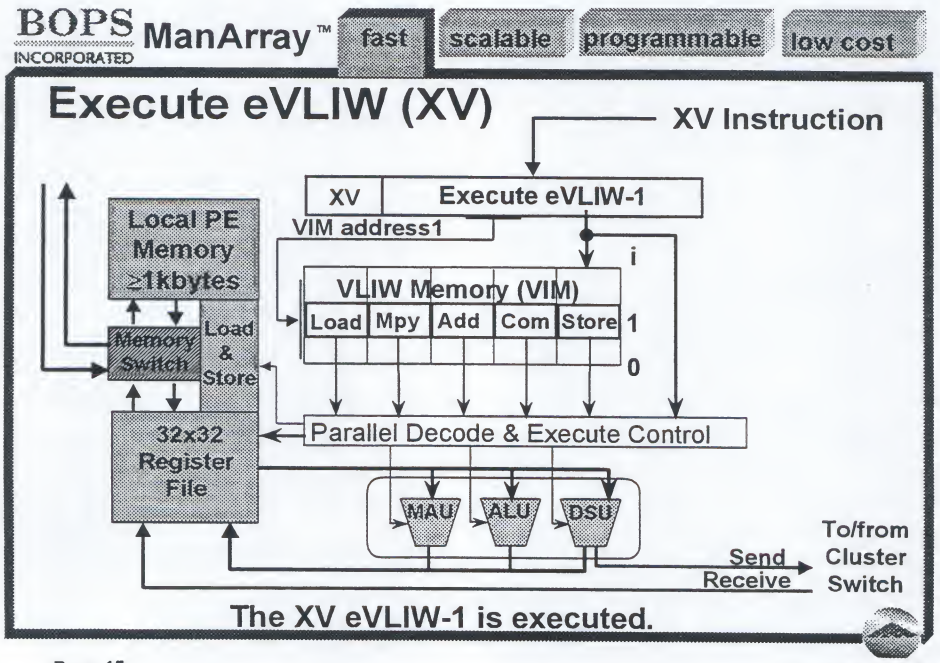
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
Execute eVLIW (XV)
XV Instruction
XV
Execute eVLIW-1
VIM address1
i
Local PE Memory ≥1kbytes
VLIW Memory (VIM)
Load
Mpy
Add
Com
Store
1
0
Memory Switch
Load & Store
32x32 Register File
Parallel Decode & Execute Control
MAU
ALU
DSU
To/from Cluster Switch
Send
Receive
The XV eVLIW-1 is executed.
Page 15
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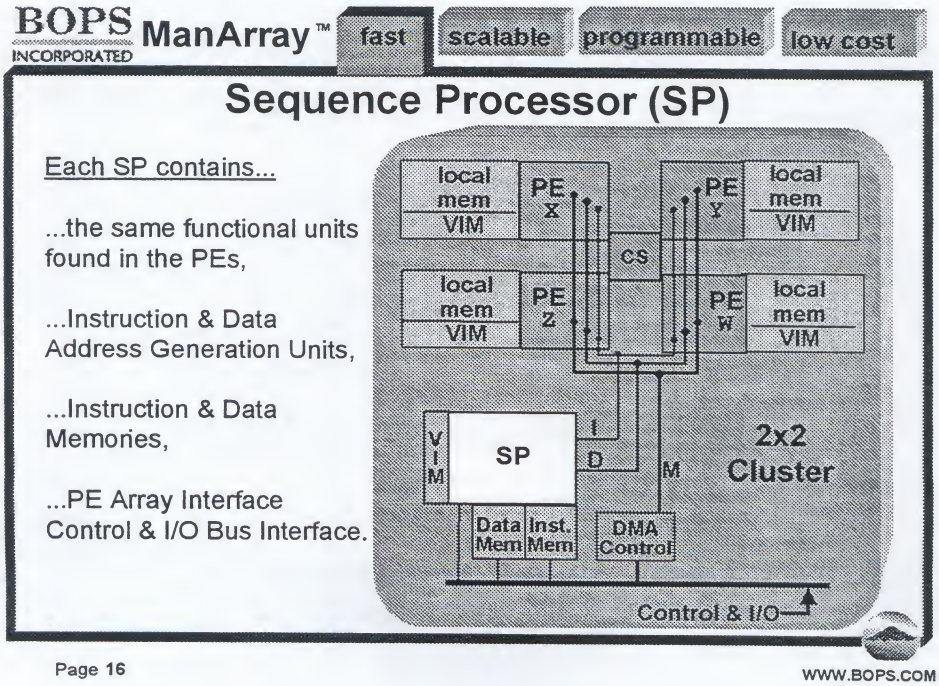
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
Sequence Processor (SP)
Each SP contains...
...the same functional units found in the PEs,
...Instruction & Data Address Generation Units,
...Instruction & Data Memories,
...PE Array Interface Control & I/O Bus Interface.
local mem VIM
PE X
PE Y
PE Z
PE W
CS
SP
VIM
I
D
M
2x2 Cluster
Data Mem
Inst. Mem
DMA Control
Control & I/O
Page 16
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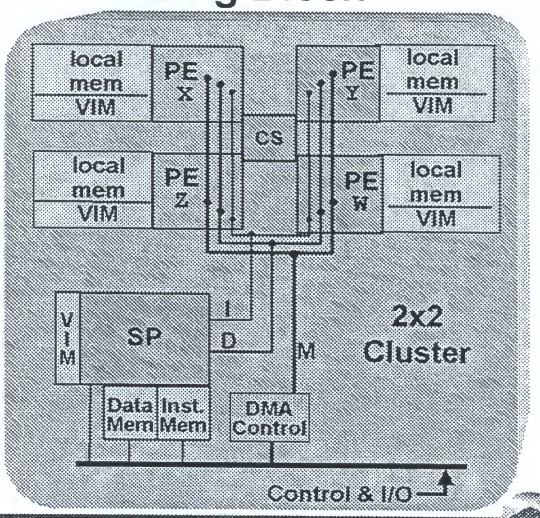
2x2 Cluster Building Block

What are PEs?
What is VIM? And how does it work?
What are SPs?

Why a 2x2 Cluster? How can you scale to larger & smaller arrays?



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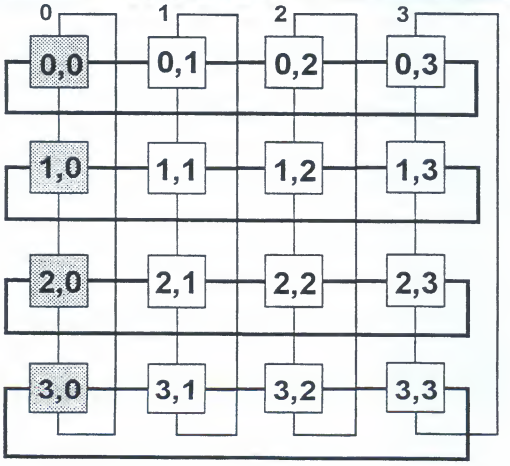
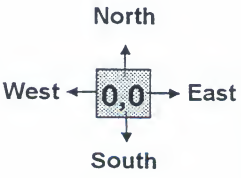
A 4x4 Torus...



Standard PE



Page 18

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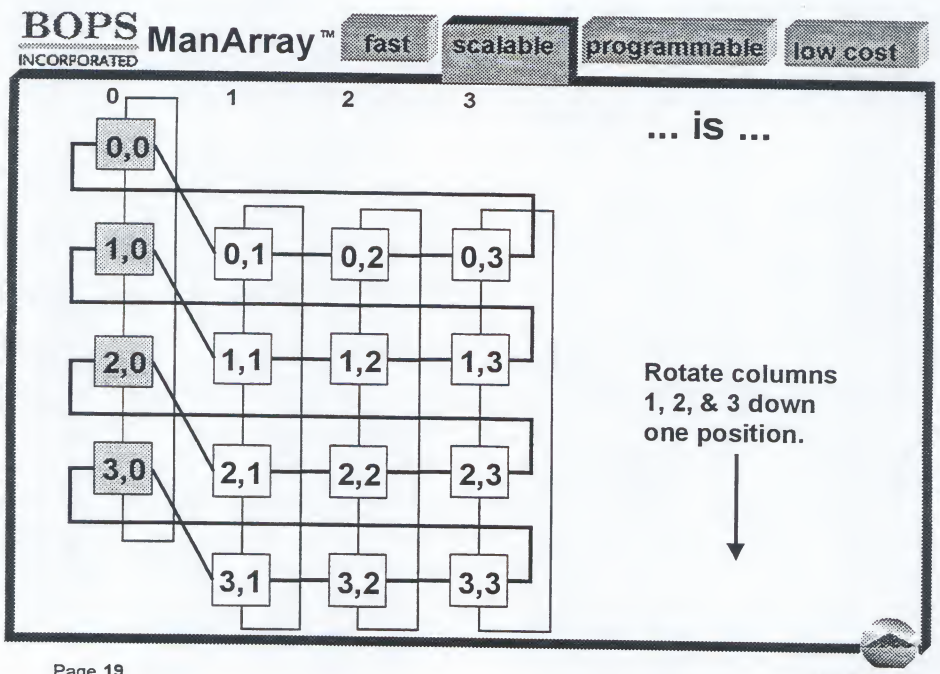
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
0
1
2
3
0,0
1,0
2,0
3,0
0,1
0,2
0,3
1,1
1,2
1,3
2,1
2,2
2,3
3,1
3,2
3,3
... is ...
Rotate columns 1, 2, & 3 down one position.
Page 19
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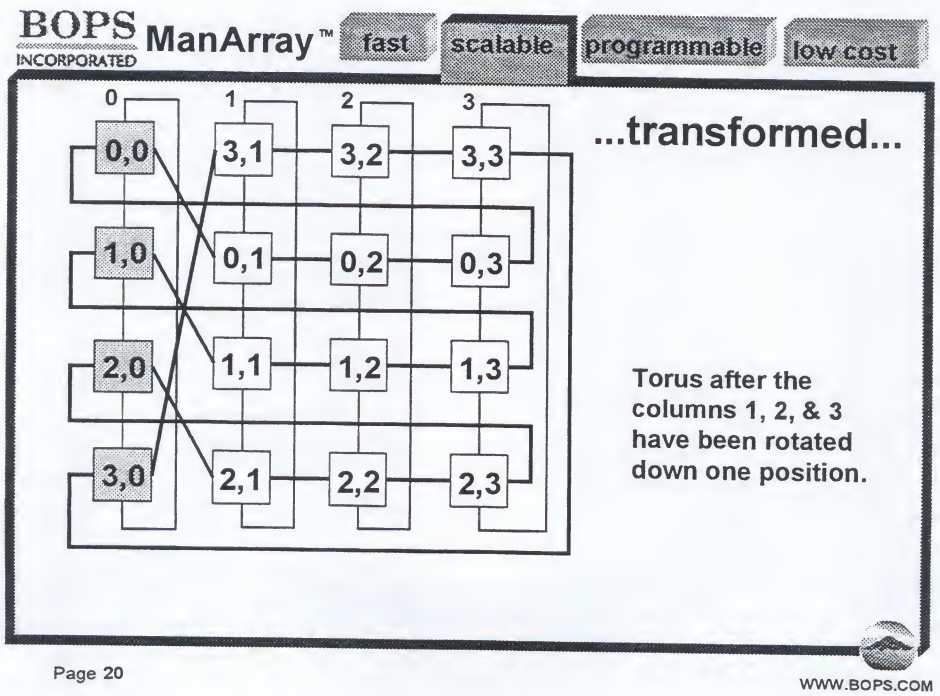
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
0
1
2
3
0,0
1,0
2,0
3,0
3,1
3,2
3,3
0,1
0,2
0,3
1,1
1,2
1,3
2,1
2,2
2,3
...transformed...
Torus after the columns 1, 2, & 3 have been rotated down one position.
Page 20
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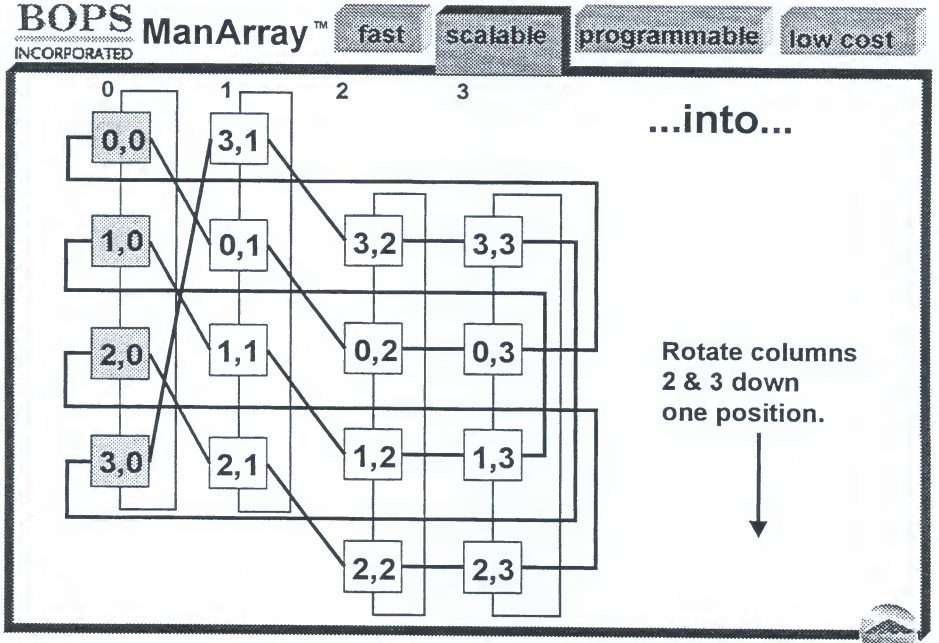
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
0
1
2
3
0,0
3,1
3,2
3,3
1,0
0,1
2,0
1,1
0,2
0,3
3,0
2,1
1,2
1,3
2,2
2,3
...into...
Rotate columns 2 & 3 down one position.
Page 21
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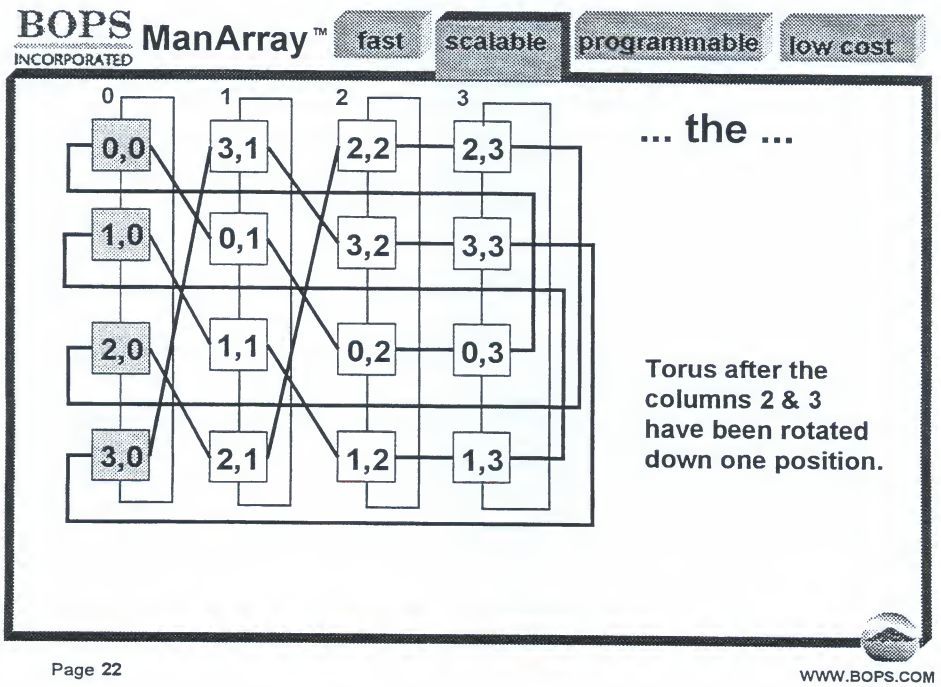
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
0
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2
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3,1
2,2
2,3
1,0
0,1
3,2
3,3
2,0
1,1
0,2
0,3
3,0
2,1
1,2
1,3
... the ...
Torus after the columns 2 & 3 have been rotated down one position.
Page 22
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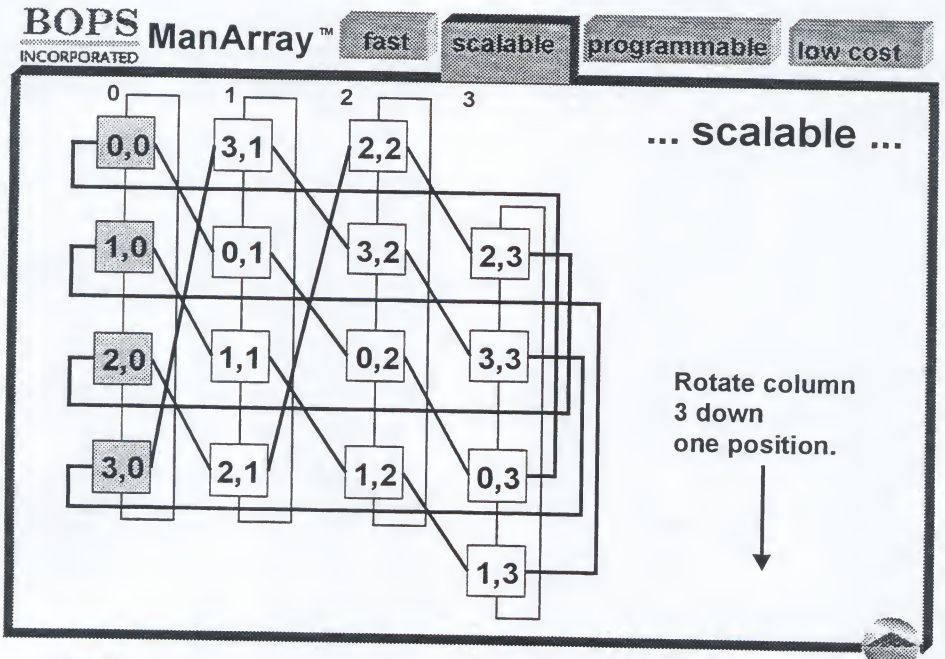
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
0
1
2
3
0,0
3,1
2,2
1,0
0,1
3,2
2,3
2,0
1,1
0,2
3,3
3,0
2,1
1,2
0,3
1,3
... scalable ...
Rotate column 3 down one position.
Page 23
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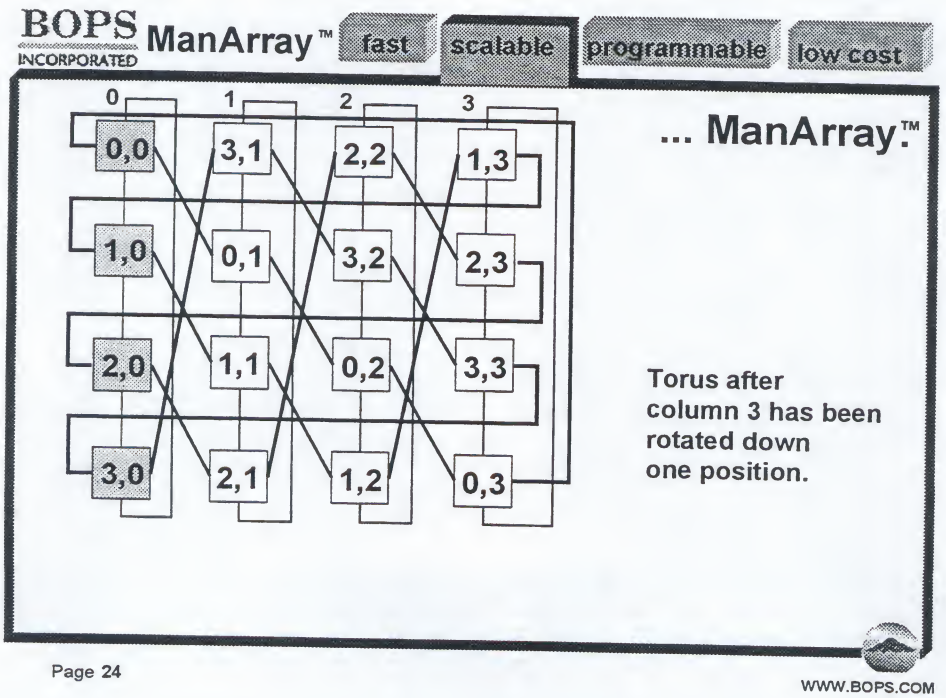
BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
0
1
2
3
0,0
3,1
2,2
1,3
1,0
0,1
3,2
2,3
2,0
1,1
0,2
3,3
3,0
2,1
1,2
0,3
... ManArray™
Torus after column 3 has been rotated down one position.
Page 24
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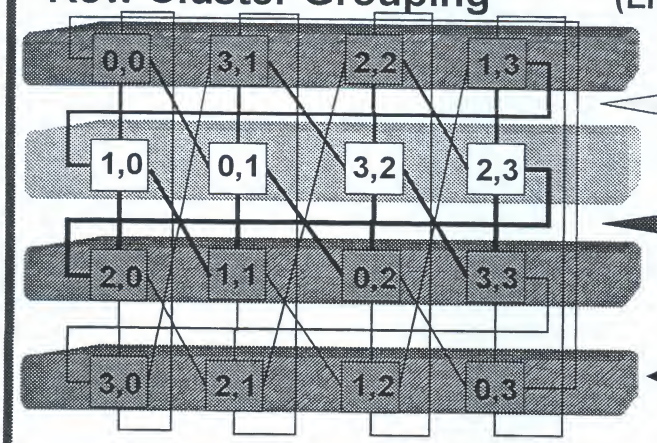
Row Cluster Grouping (Enhanced Torus)



North & West ports cross Cluster boundary here.

South & East ports cross Cluster boundary here.

Each row is a 2x2 Cluster with transpose PEs together.

To cut wiring in 1/2, combine the N/W & S/E links in SIMD!

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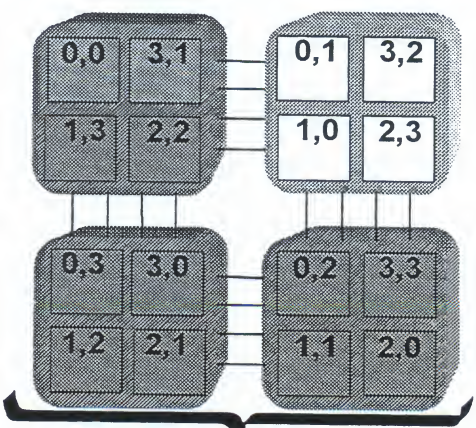
Creation of 4x4 ManArray™

Grouping the Clusters for a Regular Layout

Rearrange the 4-PE Row Clusters.

Use the shared links between the Clusters.

This rearrangement provides a regular layout for physical design.



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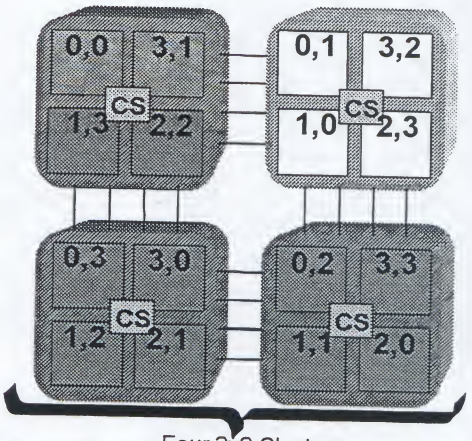
Creation of 4x4 ManArray™
Enhancing algorithm performance

Improve the connectivity of the array.

The Cluster Switch (CS) completely connects the PEs within the 4 Clusters.

The connected Clusters provide algorithmic performance advantages



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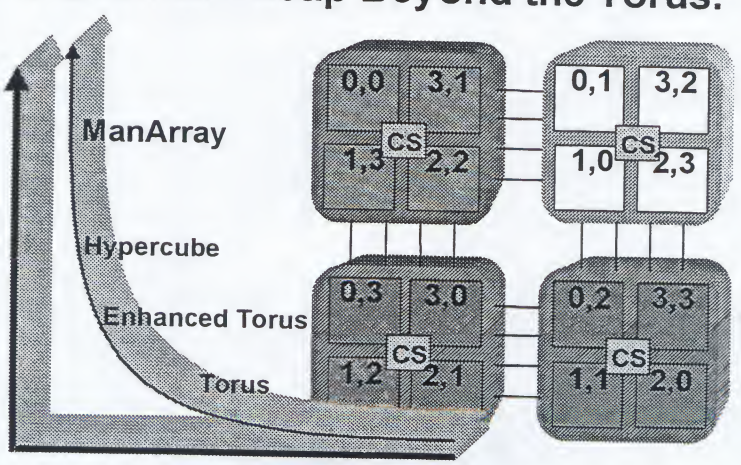
... a Quantum-Leap Beyond the Torus.



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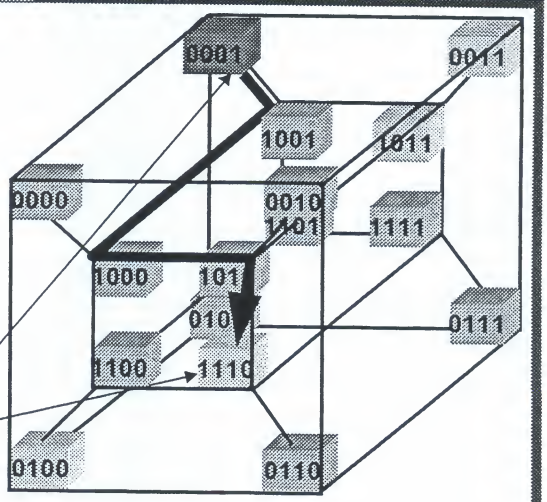
4D Hypercube

Definition

A d-Dimension hypercube has 2^d nodes.
A PE node ID is a d-bit binary string.
PEs are directly connected if & only if their IDs differ by 1-bit.

Hypercube long path
A d=4 hop long path is shown between PE-0001 & PE-1110.



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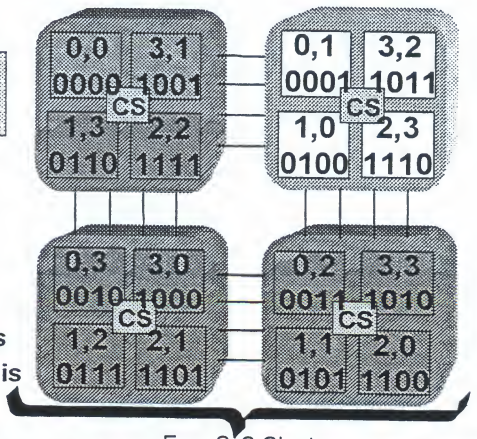
Creation of 4x4 ManArray™ Hypercube embedding:

Embed the hypercube by encoding the (i,j) PE nodes with Gray Codes.

PE-i,j
G_iG_j

Note that each cluster contains the longest hypercube paths.

In ManArray, the furthest apart hypercube nodes become Cluster neighbors and the network diameter is cut in half.



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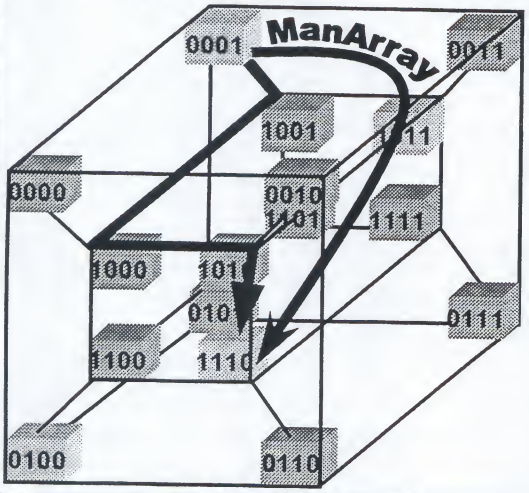
4D Hypercube = Four 2x2 Clusters



ManArray advantages

- For k-dimension hypercubes, nodes of distance k become of distance 1 on the ManArray
- All ManArray distances are $\leq \lceil k/2 \rceil$

Example applications

All-to-All Communications
Perfect Shuffle
Matrix Transposition
Matrix Multiplication
DCT/IDCT
Stockham FFT
Batcher Sort

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BOPS INCORPORATED ManArray™ fast scalable programmable low cost

Physical Attributes

- Single-cycle register-to-register transfers between PEs:
  - Within Clusters and between orthogonal Clusters
  - N,E,S,W, Hypercube, Transpose, HyperComplement, ...
- Enhanced connectivity with 1/2 wires between Clusters
- PEs are completely connected in the Clusters
- Only 2 ports required per PE independent of the topology
- PEs decoupled from the topology
- No global wrap-around wires
- Regular layout for physical design
- Built-in scalability: 1x1, 1x2, 2x2, 2x4, 4x4, 4x4x4 cores

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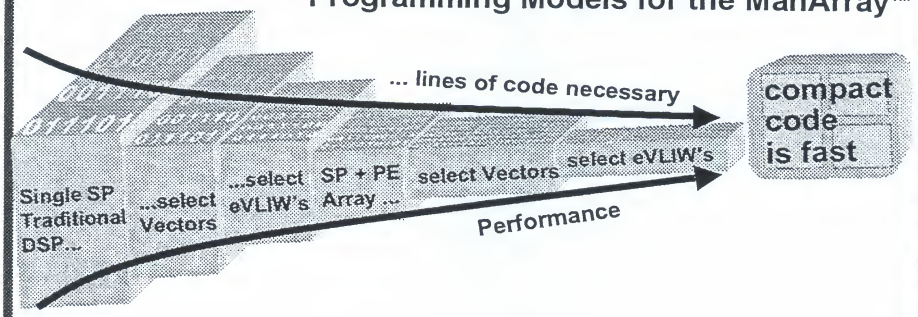
BOPS INCORPORATED ManArray™ fast scalable programmable low cost

Programming Models for the ManArray™



- Programmers increase their code density as they move from traditional programming models towards fully optimized eVLIW code
- Programmers can select any of these models to run independently
- Optimized library of algorithms targeting 3D graphics, MPEG encoding, audio, communications, signal processing ...

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BOPS INCORPORATED ManArray™ fast scalable programmable low cost

One Example Appropriate for Many Applications

(4x4 Matrix) x (4x4 Matrix) Multiplication (16-bit data)

- → 144 Operations per matrix multiply (64mpys+48adds+load16/store16)
- → 96 Cycles; 1 BOPS Sequence Processor(SP) using multiply-adds
- → 72 Cycles; 1 BOPS SP using dual 16-bit packed data formats
- → 32 Cycles; 1 BOPS SP using dual 16-bit packed data & eVLIW
- → 8 Cycles; 2x2 array using dual 16-bit packed data & eVLIWs
- → 2 Cycles; 4x4 array using dual 16-bit packed data & eVLIWs

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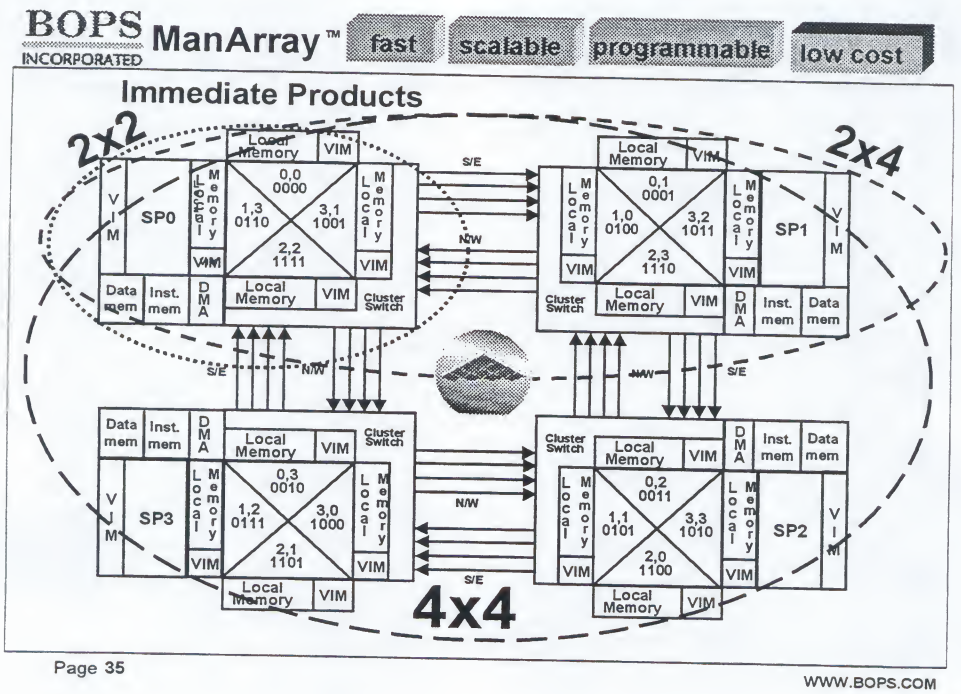
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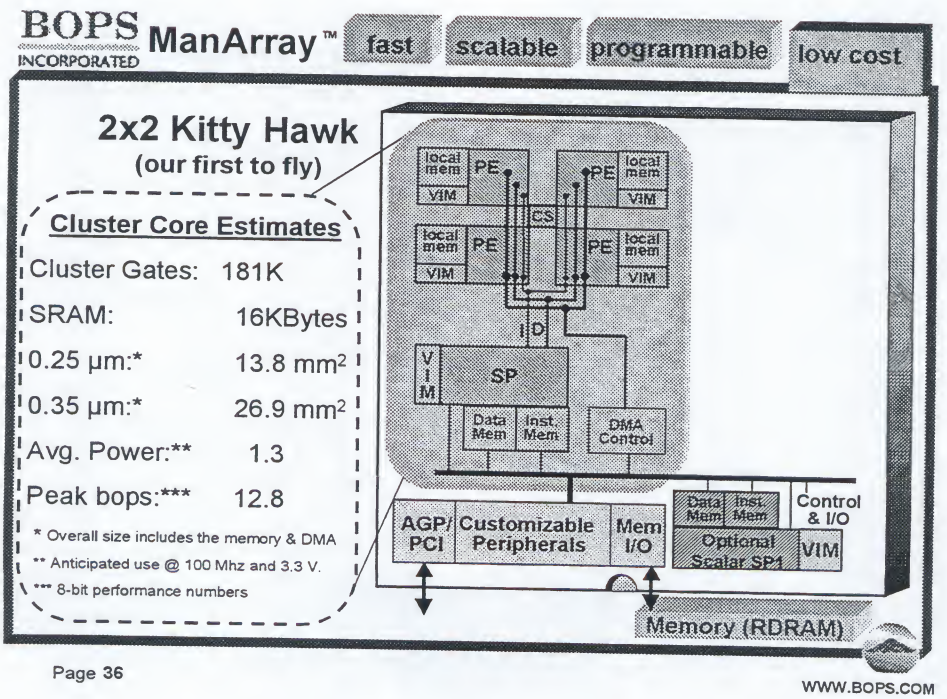
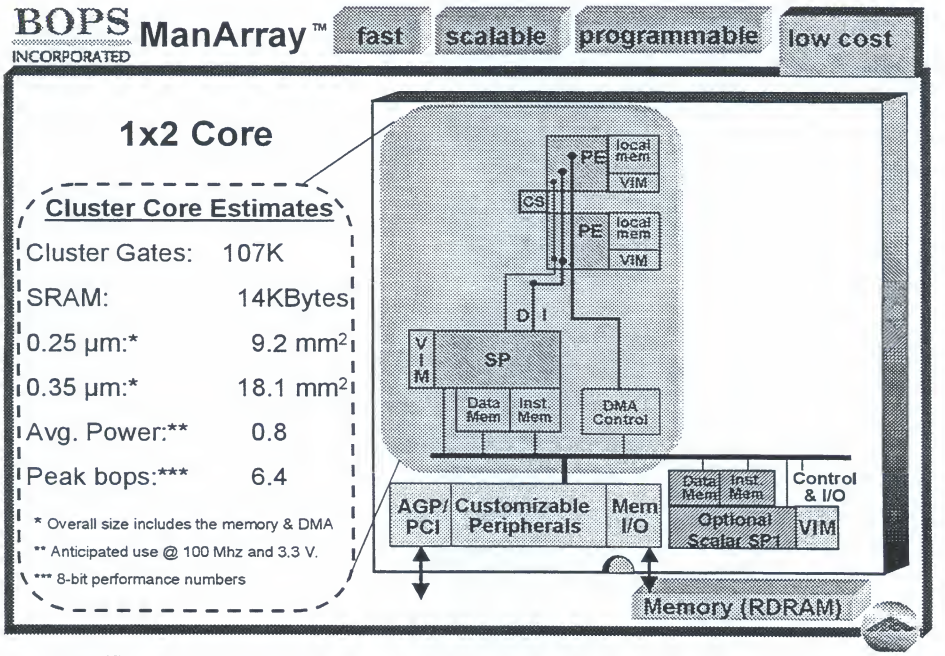
ManArray™
fast
scalable
programmable
low cost
Immediate Products
2x2
2x4
4x4
SP0
SP1
SP2
SP3
Local Memory
VIM
Data mem
Inst. mem
DMA
Cluster Switch
S/E
N/W
0,0 0000
1,3 0110
3,1 1001
2,2 1111
0,1 0001
1,0 0100
3,2 1011
2,3 1110
0,3 0010
1,2 0111
3,0 1000
2,1 1101
0,2 0011
1,1 0101
3,3 1010
2,0 1100


BOPS INCORPORATED
ManArray™
fast
scalable
programmable
low cost
2x2 Kitty Hawk
(our first to fly)
Cluster Core Estimates
Cluster Gates: 181K
SRAM: 16KBytes
0.25 µm:* 13.8 mm²
0.35 µm:* 26.9 mm²
Avg. Power:** 1.3
Peak bops:*** 12.8
* Overall size includes the memory & DMA
** Anticipated use @ 100 Mhz and 3.3 V.
*** 8-bit performance numbers
local mem
PE
VIM
CS
I/O
SP
Data Mem
Inst. Mem
DMA Control
AGP/ PCI
Customizable Peripherals
Mem I/O
Control & I/O
Optional Scalar SP1
Memory (RDRAM)



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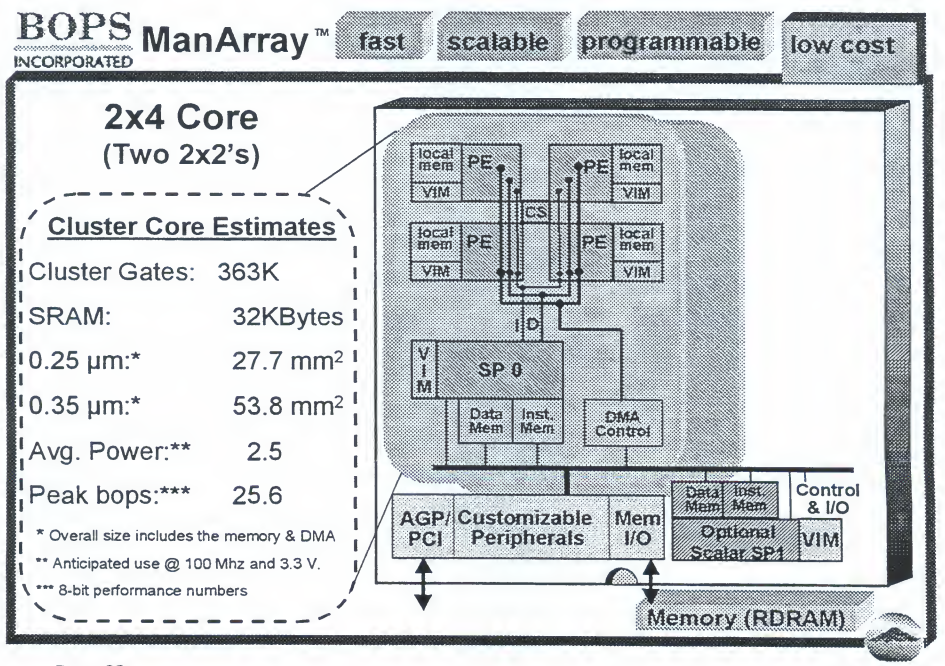

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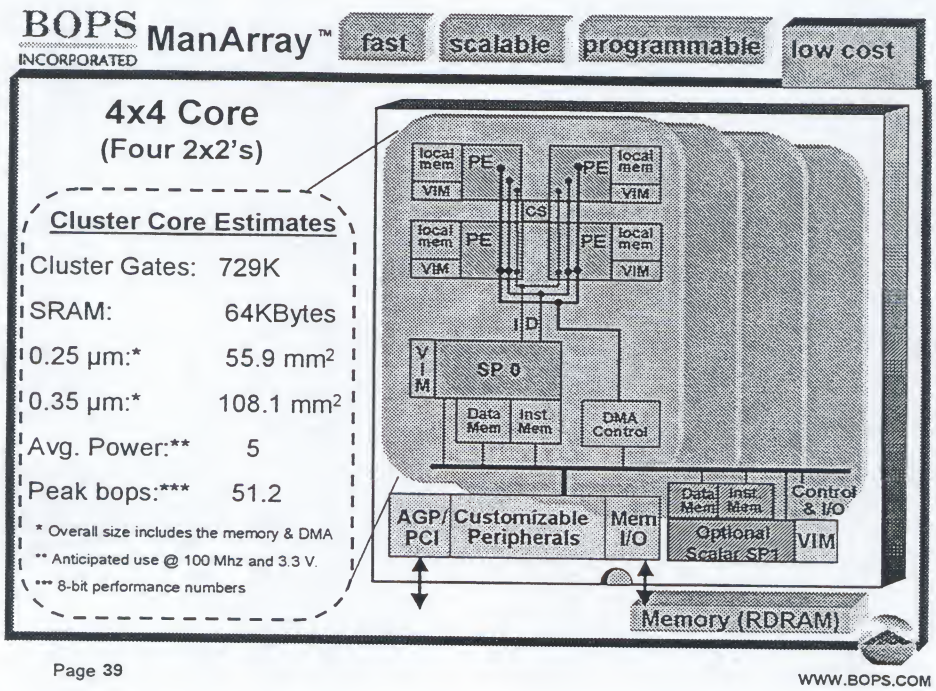

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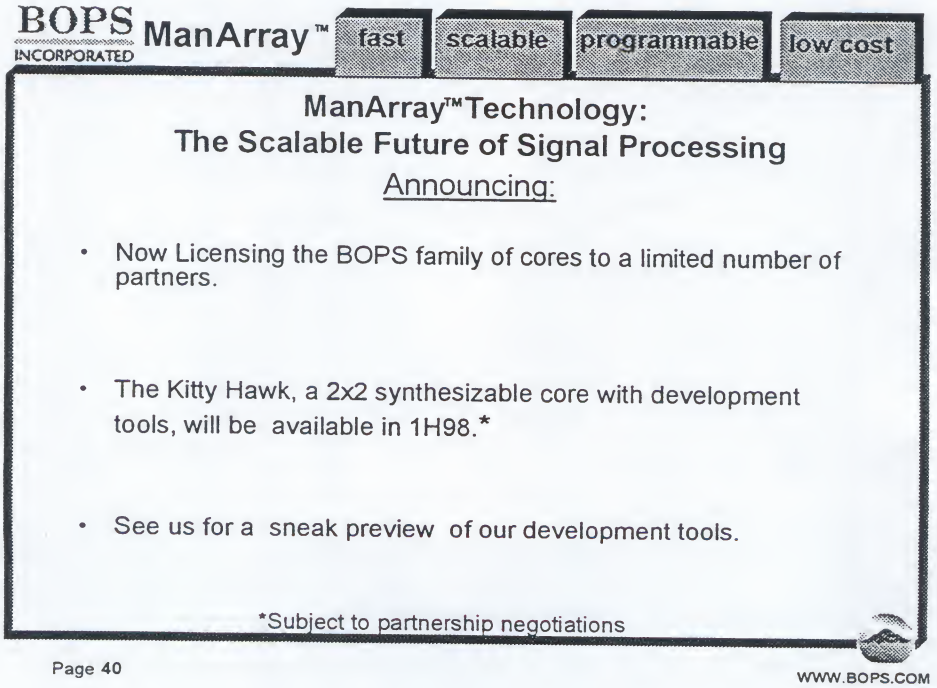

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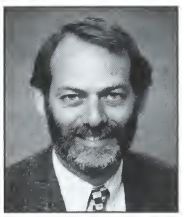

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VOLUME 11, NUMBER 11
AUGUST 25, 1997

MICROPROCESSOR REPORT

THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

National Semi Acquires Cyrix

Cyrix Gains Licensed Fab; National Touts PC on a Chip

by Linley Gwennap

This article is an expanded and updated version of the news flash distributed with our last issue.

National Semiconductor has leapt into the PC processor market by acquiring x86 vendor Cyrix for an estimated $550 million in stock. The deal positions the combined company as a stronger force in the PC processor market, bringing Cyrix's x86 designers together with National's fab capacity. National recently opened a 0.35-micron fab, competitive with the best process technology that Cyrix is getting from its current foundry, IBM. National also holds the essential Intel patent cross license agreement that will allow it to legally manufacture and sell Intel-compatible processors.

From National's standpoint, the deal allows it to extend its line of PC-on-a-chip products, currently embodied by its NS486 processor (see MPR 9/11/95, p. 1). The Cyrix processors will provide more powerful cores for future highly integrated products. National CEO Brian Halla envisions a future in which PC-compatible "appliances" sell for $500 or even $250, with tubes of these low-cost devices for outstripping those of traditional PCs.

How these two strategies will play together in the long term is unclear. The initial press announcement was somewhat schizophrenic, with Cyrix stressing head-to-head competition with Intel while National hosted in on the PC-on-a-chip concept. We expect the new company to pursue both strategies for an initial period, but after a couple of years it may choose to focus on one or the other.

Halla Revitalizes National's Fab Technology

Under former CEO Gil Amelio, National's fab technology had languished; as recently as 1995, National's best process was 0.8-micron (drawn), while many other chip vendors were putting 0.35-micron processes into production. Amelio's cost-cutting measures left little funding for expensive new fabs. In the fall of 1995, National did break ground on a new fab in South Portland, Maine, but continued funding problems slowed progress on the new facility.

After Amelio left to take over Apple in January 1996, Halla took charge at National and immediately gave the green light for the Portland project to proceed at full speed. He also expanded the size of the facility significantly, boosting the total investment to more than $1 billion over three years. The Portland fab went from shovel to sample silicon in 18 months, and National will begin shipping production parts from the new fab next month.

National also vastly increased funding for IC process development, hiring many experienced hands to accelerate development of a 0.35-micron process. Halla wanted the Portland fab to deploy the 0.35-micron process when it opened, with a goal of reaching the 0.25-micron level in 1998 and 0.18-micron in 1999. After spending $70 million for process development in 1996 and an expected $100 million this year, National has met its initial goal, the first production parts from the Portland fab are being built in a 0.35-micron (effective) CMOS process.

National hopes to make a fast transition to the 0.25-micron level. The initial process is designed such that 70% of the equipment can also be used to build 0.25-micron parts; this high degree of commonality should smooth the transition. The company expects the 0.25-micron process to be fully qualified in its Santa Clara (Calif.) development fab by December, with volume production in Portland around the middle of 1998—still a year behind the industry leaders.

Plenty of Capacity for Cyrix Parts

Halla clearly has big plans for the Portland fab. By the end of 1999, the fab will be built out to a capacity of 7,000 wafers per week, roughly the size of AMD's Fab 25 or Intel's largest fabs. This capacity will easily support a doubling or tripling of Cyrix's market share in addition to National's current products. If necessary, the entire fab could be devoted to x86 chips; National's other products can be fabricated offshore through an existing arrangement with foundry TSMC.

National also intends to maintain Cyrix's existing relationship with IBM, which currently manufactures chips for

Continued on page 6

Inside: Intel Sues Digital, Buys Chips ◇ Slot 2 ◇ 440LX ◇ Retrospective

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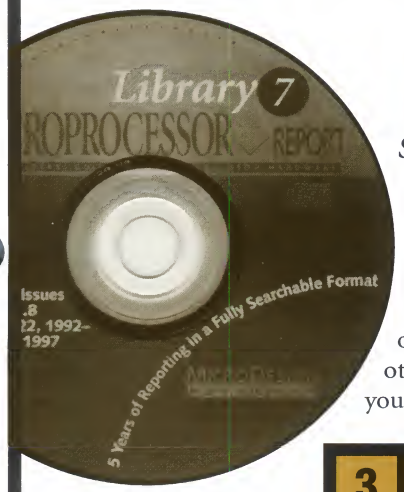
Microprocessor Report has been the leading technical publication for the microprocessor industry since it was first introduced by Michael Slater in 1987. Published 17 times a year, *Microprocessor Report* is an independent, exclusively subscriber-based publication focused on the constant advances in microprocessor technology.

Written by engineers for a technically astute audience, you'll find:

- New microprocessor announcements and reviews of new chips
- In-depth analysis of microprocessor architectures and implementations
- The microprocessor implications of emerging platforms
- Emerging personal computer technologies, workstation designs, handheld system architectures, embedded processors, DSP technology, and intellectual property issues



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3 Technical Library

The most knowledgeable decision makers in the microprocessor industry are continually challenged by new technologies, conflicting claims, and emerging trends. MDR's Technical Library and Special Reports help clarify choices by providing in-depth exploration of key issues and the technologies driving the industry.

Beyond Conventional 3D: Talisman and Other Advanced Architectures

Peter N. Glaskowsky, senior PC analyst, MDR

NEW RELEASE!

Expected release date: October, 1997

Interest in 3D graphics is exploding, but conventional architectures are already starting to run out of gas. To continue the rapid pace of 3D performance advances (doubling performance every six months), radical new approaches will be needed as early as next year. Microsoft's Talisman is one such approach, but others are offering competing designs that may win out.

Beyond Conventional 3D first describes the basic technical concepts of the conventional PC 3D pipeline. It then offers an insightful exploration of the most promising opportunities for enhanced quality and performance, and which companies are likely to deliver on them.

In nearly 100 pages, you'll find:

- Objective metrics to compare 3D architectures including display quality, rendering speed, and chip complexity
- An exploration of alternatives to the conventional PC pipeline, including Microsoft's Talisman and HP PixelFlow
- Specific techniques to improve display quality, such as increased resolution, color depth, and polygon precision; lighting and texture enhancements and more
- An analysis of market conditions that will predispose some companies to succeed, others to collapse

MDR Technical Library

Intel's Merced and IA-64: Technology and Market Forecast

Linley Gwennap, publisher and editor in chief, **Microprocessor Report**

NEW RELEASE!

Even as competition for x86 processors reaches a peak, Intel is readying its next generation of microprocessors based on the architecture codeveloped with Hewlett-Packard, dubbed IA-64. Intel's goals for Merced, the first IA-64 processor, are simple: to deliver the fastest processor in the world for high-end workstations and servers, providing a strong new competitor for the RISC vendors that dominate those markets today. Over time, IA-64 is likely to filter down into the PC market as well, ultimately displacing x86.

Can IA-64 deliver on its promise? In the first detailed technical report on the subject, Intel expert Linley Gwennap looks at:

- IA-64 design philosophy, including IC technology, system design, and rationale for a new ISA
- IA-64 software model and its combination of two instruction sets in one processor
- Details of IA-64's 64-bit extensions including instruction formats, branching behavior, and operation grouping
- MDR's forecast for Merced including clock speed, die size, and peformance
- MDR's projected roadmap for Intel's IA-64 processor family

Expected release date: November, 1997

Battle for the Desktop: Strategies for x86 Microprocessors

Michael Slater, founder and editorial director, MDR

NEW RELEASE!

The next twelve months promise one of the most competitive and demanding markets for x86 processors, with AMD, Cyrix/National, and IDT/Centaur all offering viable alternatives to Intel. But in the battle for the desktop, can these alternatives attain a sustainable, profitable market share? This insightful analysis by Michael Slater gives you detailed information on the products and strategies of each x86 vendor. It covers key issues such as the ability of Intel's competitors to maintain Socket 7's viability in the face of Intel's move to Slot 1, and the role of instruction set extensions beyond MMX.

Battle for the Desktop gives you a detailed review of the shifting PC environment with its changing user demands, unique market segments, and future trends. It then lays out Intel's and each x86 competitor's chips and processor roadmap against the market demands and the offerings of the other companies. For each x86 player, you'll get:

- Corporate histories and key statistics
- Customers
- Fab capacity
- Legal strategy
- Roadmaps
- Detailed descriptions of the processors themselves

Expected release date: December, 1997

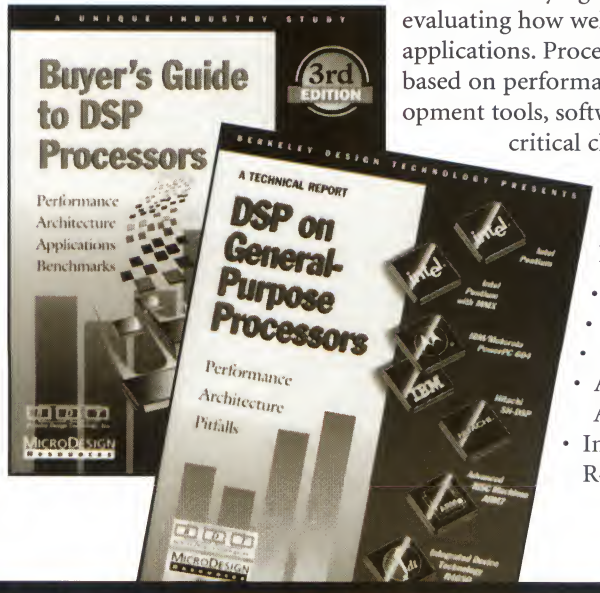
Buyer's Guide to DSP Processors, 3rd Edition

Berkeley Design Technology

Fully updated and revised, this guide to digital-signal processors provides key insights into each processor's strengths and weaknesses, as well as complete tables to directly compare processors for particular features or performance metrics. Written by DSP experts, Berkeley Design Technology, this report evaluates processor performance based on BDT's own benchmarks.

Processors evaluated include:

- Texas Instruments TMS320C62xx
- Motorola DSP563xx
- Motorola DSP566xx
- Motorola DSP568xx
- Analog Devices ADSP-21 cspxx
- Plus 14 other processor families



DSP on General-Purpose Processors

Berkeley Design Technology

In this unique report, Berkeley Design Technology analysts examine today's general-purpose processors, evaluating how well they meet the needs of DSP applications. Processors are objectively evaluated based on performance, architecture, pitfalls, development tools, software, price, and packaging—critical characteristics to help you decide which is best for your application.

Processors evaluated include:

- Intel Pentium with MMX
- IBM/Motorola PowerPC 604
- Hitachi SH-DSP
- Advanced RISC Machines ARM7
- Integrated Device Technology R4650

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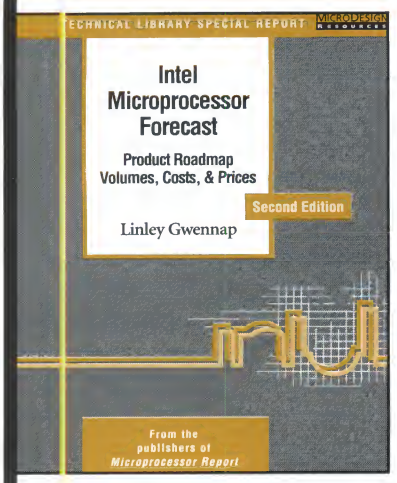
Intel Microprocessor Forecast, 2nd Edition

Linley Gwennap, publisher and editor in chief, Microprocessor Report

Short of sitting in on an Intel microprocessor strategy meeting, you just cannot get a better look at Intel's plans and potentials.



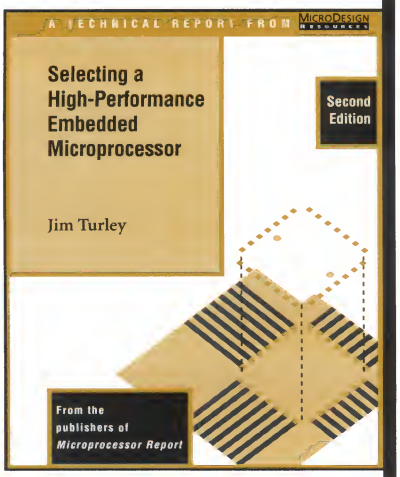
Whether you compete or collaborate with Intel, you need solid data on where the industry's most powerful semiconductor firm is headed. In nearly 100 pages of text, charts, and figures (all in full color), you'll find the most detailed forecast available of Intel's manufacturing capacity and costs, product roadmap, pricing, and unit shipments.

Intel Microprocessor Forecast, 2nd Edition, provides the details that strategists, investors, and decision-makers need in order to plan for upcoming changes in the Intel product mix. You'll find:

- Schedule and performance estimates for Katmai, Willamette, Deschutes, and Merced (IA-64)
- Manufacturing cost estimates for current and future Intel processors
- Price forecasts through the end of 1998
- Unit shipment forecasts through the end of 1999

Selecting a High-Performance Embedded Microprocessor, 2nd Edition

Jim Turley, senior editor, Microprocessor Report



Some of the fastest, most complex, and highest volume chips have been designed for embedded applications. Which is right for yours? With more than 100 32-bit embedded microprocessors to choose from, it can take months to find the right one. That's why the fully revised and updated second edition of *Selecting a High-Performance Embedded Microprocessor* is such a valuable decision-making resource.

This 450-page volume, filled with easy-to-use graphs, tables, and charts that compare performance, costs, and power consumption, is an indispensable time saver and guide. You'll find:

- Analysis and specifications for over 115 chips and 17 architectures including reviews of the latest chips like picoJava, PowerPCs and more. Every chip is analyzed based on the metrics you're most likely to need: cost, performance, power requirements, availability, and prospects
- Processor selection guides which make it easy to find chips that meet your specifications
- Independent analysis of each architecture from the most trusted source in the industry

New DRAM Technologies: A Comprehensive Analysis of the New Architectures, 2nd Edition

Steven Przybylski, Ph.D.

This one-of-a-kind, comprehensive resource is designed to help you understand the DRAM choices and trends that are moving DRAM technology to new performance peaks. The second edition delivers an expert analysis of system-level implications, side-by-side architecture comparisons, and a historical perspective.

You'll find:

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- A new metric to compare DRAM architectures
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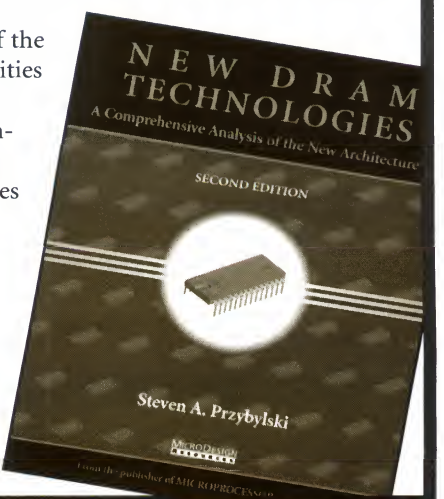
- Changes, directions, and opportunities in the 64-Mb generation of DRAM and new challenges at the 256-Mb and 1-Gb levels
- Detailed discussion of the ongoing incompatibilities among SDRAMs
- Analysis of the system-level impact of high-performance memories with and without secondary cache
- Thorough tutorial material, including: what DRAMs are, how they work, and how they are used together to form memory systems



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- Shows transistor count for each processor
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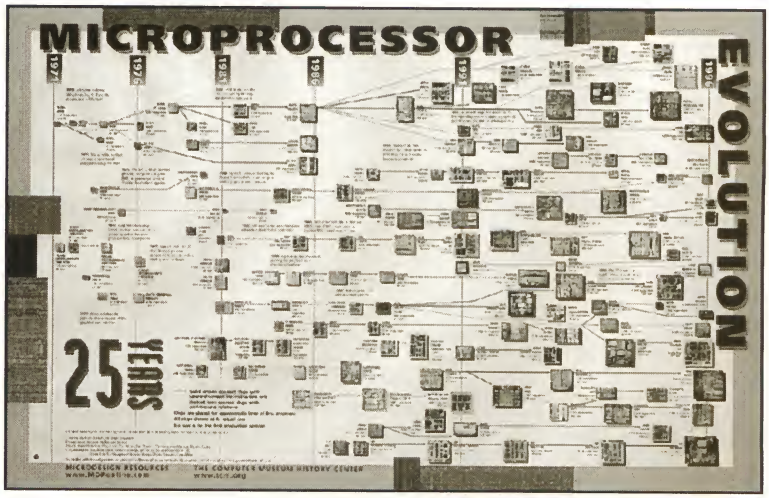

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